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Dual-frequency single-inductor multiple-output (DF-SIMO) power converter topology for SoC applications

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Dual-frequency single-inductor multiple-output (DF-SIMO)

power converter topology for SoC applications

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To Yaya, Ziyi, and my parents

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ABSTRACT

Modern mixed-signal SoCs integrate a large number of sub-systems in a single nanometer CMOS chip. Each sub-system typically requires its own independent and well-isolated power supply. However, to build these power supplies requires many large off-chip passive components, and thus the bill of material, the package pin count, and the printed circuit board area and complexity increase dramatically, leading to higher overall cost. Conventional (single-frequency) Single-Inductor Multiple-Output (SIMO) power converter topology can be employed to reduce the burden of off-chip inductors while producing a large number of outputs. However, this strategy requires even larger off-chip output capacitors than single-output converters due to time multiplexing between the multiple outputs, and thus many of them suffer from cross coupling issues that limit the isolation between the outputs.

In this thesis, a Dual-Frequency SIMO (DF-SIMO) buck converter topology is proposed. Unlike conventional SIMO topologies, the DF-SIMO decouples the rate of power conversion at the input stage from the rate of power distribution at the output stage. Switching the input stage at low frequency (~2 MHz) simplifies its design in nanometer CMOS, especially with input voltages higher than 1.2 V, while switching the output stage at higher frequency enables faster output dynamic response, better cross-regulation, and smaller output capacitors without the efficiency and design complexity penalty of switching both the input and output stages at high frequency. Moreover, for output switching frequency higher than 100 MHz, the output capacitors can be small enough to be integrated on-chip. A 5-output 2-MHz/120-MHz design in 45-nm CMOS with 1.8-V input targeting low-power microcontrollers is presented as an application. The outputs vary from 0.6 to 1.6 V, with 4 outputs providing up to 15 mA and one output providing

up to 50 mA. The design uses single 10-μH off-chip inductor, 2-nF on-chip capacitor for each 15-mA output and 4.5-nF for the 50-mA output. The peak efficiency is 73%, Dynamic Voltage Scaling (DVS) is 0.6 V/80 ns, and settling time is 30 ns for half-to-full load steps with no observable overshoot/undershoot or cross-coupling transients. The DF-SIMO topology enables realizing multiple efficient power supplies with faster dynamic response, better cross-regulation, and lower overall cost compared to conventional SIMO topologies.

CHAPTER 1

INTRODUCTION

Many low-power mixed-signal System-on-Chip (SoCs), such as microcontrollers, employ a single-output buck converter to create an efficient low-voltage power supply (1.2 V or less) for their low-power digital core (less than 50-mA load) out of a 1.8-V input supply as shown in Fig. 1.1. However, the slow dynamic response of such converter impedes the effective use of Dynamic Voltage Scaling (DVS) to reduce the power consumption of the digital core [1]–[11]. Moreover, many other modules, such as memory, data converters, and other analog functions require their own power supplies. These are typically realized using fully-integrated linear regulators to avoid the additional off-chip passives, package pins, and Printed Circuit Board (PCB) area resulting from using several buck converters. This further reduces the overall efficiency and increases the power consumption. Conventional (single-frequency) Single-Inductor Multiple-Output (SIMO) topologies [12]–[20] can be used to leverage the existing off-chip inductor to implement the additional power supplies needed by the system with better efficiency than linear regulators. However, their time-multiplexed power distribution results in poor cross regulation between the multiple power supplies, and even slower output dynamic response and larger off-chip output capacitors than single-output topologies.

This thesis proposes the Dual-Frequency SIMO (DF-SIMO) topology as an alternative to conventional SIMO topologies for implementing the multiple efficient power supplies required for systems similar to Fig. 1.1, while eliminating all off-chip capacitors as shown in Fig. 1.2, and achieving significantly faster dynamic response and better cross-regulation. This is accomplished

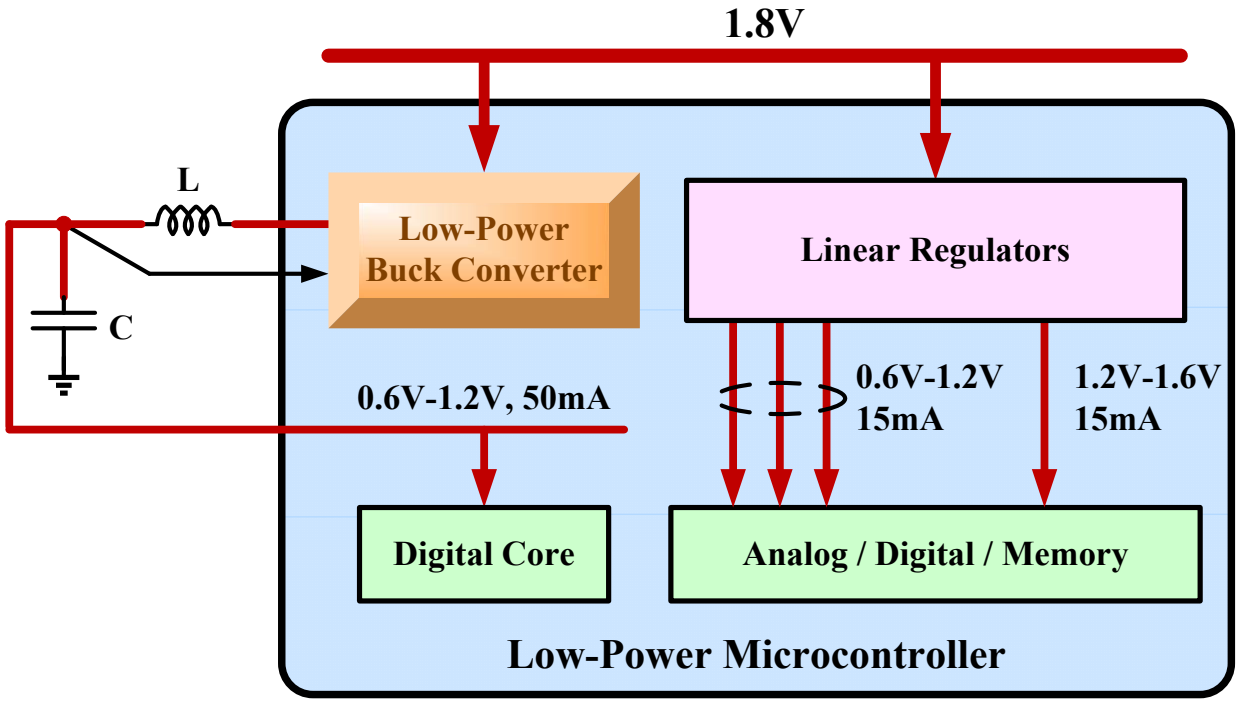


Figure 1.1. A block diagram showing the typical powering scheme of low-power microcontrollers with a single-output buck converter for the digital core and linear regulators for all other modules.

by raising the switching frequency of the output stage in the SIMO topology to beyond 100 MHz, while retaining a low input switching frequency (~2 MHz). Using high-frequency comparator-based control with a single freewheeling switch at the output stage to regulate the output voltages, along with low-frequency Pulse Width Modulation (PWM) control at the input stage to regulate the freewheeling current, the proposed topology results in an output dynamic response, cross-regulation behavior, and output capacitors sizes that are determined by the high switching frequency of the output stage rather than the input stage's low switching frequency. Thus, excessive switching losses that would result from switching the entire converter at high frequency to achieve the same performance are avoided. Moreover, low input switching frequency enables using thick-gate 1.8-V rated transistors in nanometer CMOS nodes as power

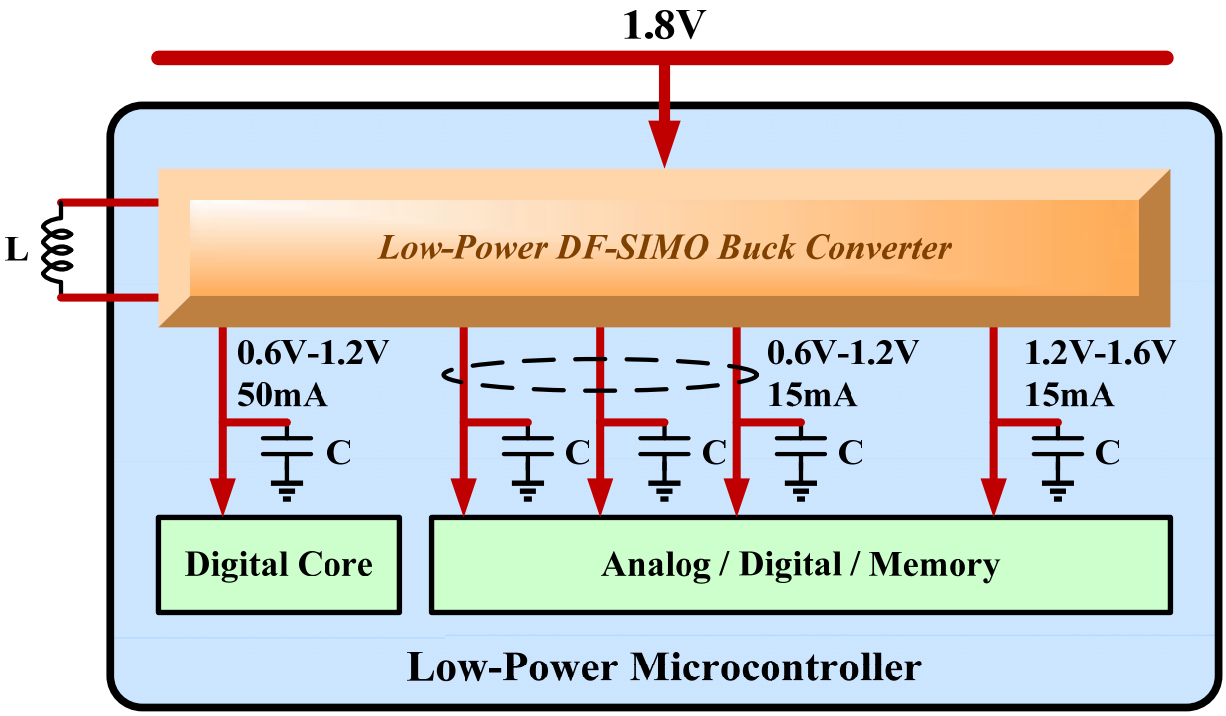


Figure 1.2. The powering scheme using the proposed DF-SIMO with fully-integrated outputs.

switches to operate the converter from 1.8 V without compromising efficiency or transistor reliability, which greatly simplifies the design of the input stage. If integrating the output capacitors is not the goal, the DF-SIMO concept can also be used with an output switching frequency that is only a few times the input switching frequency to improve the dynamic and cross-regulation behavior and reduce the off-chip capacitors of conventional SIMO topologies.

The thesis is organized as follows: chapter 2 introduces several conventional SIMO topologies and their advantages and disadvantages. Chapter 3 presents the operation principle of the DF-SIMO topology and its design tradeoffs. Chapter 4 presents the control loop small-signal analysis. Chapter 5 and 6 present the design and measurement results of a low-power dual-frequency single-inductor 5-output buck converter in 45-nm CMOS technology. The thesis is concluded in chapter 7 with possible future extension.

CHAPTER 2

OVERVIEW OF CONVENTIONAL SIMO TOPOLOGIES

Since a switching buck converter is commonly used to generate the power supply for the digital core of a mixed-signal SoC, it makes sense to leverage the existing off-chip inductor to implement the additional power supplies needed by the system. Thus, SIMO DC-DC converters shown in Fig. 2.1 offer an attractive and practical solution with less off-chip passives than multiple single-output DC-DC converters, and better efficiency than linear regulators. The basic idea behind any SIMO converter is to share the magnetic energy stored in the single off-chip inductor between all the output loads. In order to switch the current flowing through the inductor from one load to the other, a Time Multiplexing (TM) control principle is typically employed according to the voltage setting and current demand from each output load. Several schemes have been presented in the literature to control the process of cycling the inductor current into the output capacitors such that regulation is achieved [12]–[18]. In [12], nested pulse width modulation (PWM) generators are used to control the energy distribution for dual-output buck converters. The work in [15] presents a PLL-based 6-output buck converter with modified bang-bang control to achieve high stability. In [17], a 5-output buck converter is regulated by adaptively controlling the duty cycle of the freewheeling period to solve the cross-coupling issue between each output. A ripple-based adaptive off-time control is presented in [18] to regulate a 4-output buck converter which can realize faster DVS. Besides, there are some other control schemes used to implement SIMO boost converters [19], [20]. The following sections will review these schemes and discuss their advantages and disadvantages.

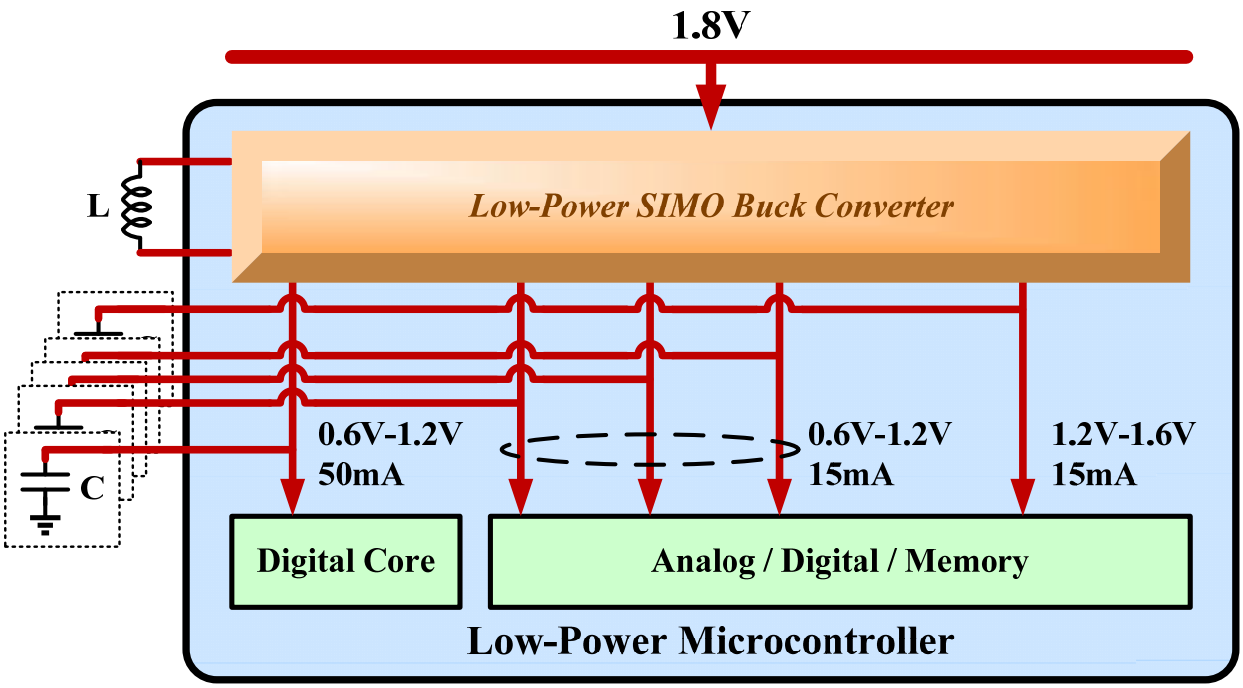


Figure 2.1. The powering scheme using the conventional SIMO converter for all the modules.

2.1 Nested PWM Control SIMO Buck Converters

As mentioned before, all SIMO converters utilize time-multiplexing control principle to steer the inductor current to each output. Fig. 2.2 shows a typical timing diagram of the inductor current for a dual-output case. It should be noted that the peak inductor current could happen before or after the load switching. In order to regulate each output separately, extra power switches are needed on the output stage. Thus, two sets of switching control signals are necessary, one for the output power distribution switches and the other for the input power generation switches. The control circuits should use the output error signals to form several local feedback loops for the output stage and a global feedback loop for the input stage. In [12], [41], two nested conventional PWM loops driven by the two output voltage errors is presented as

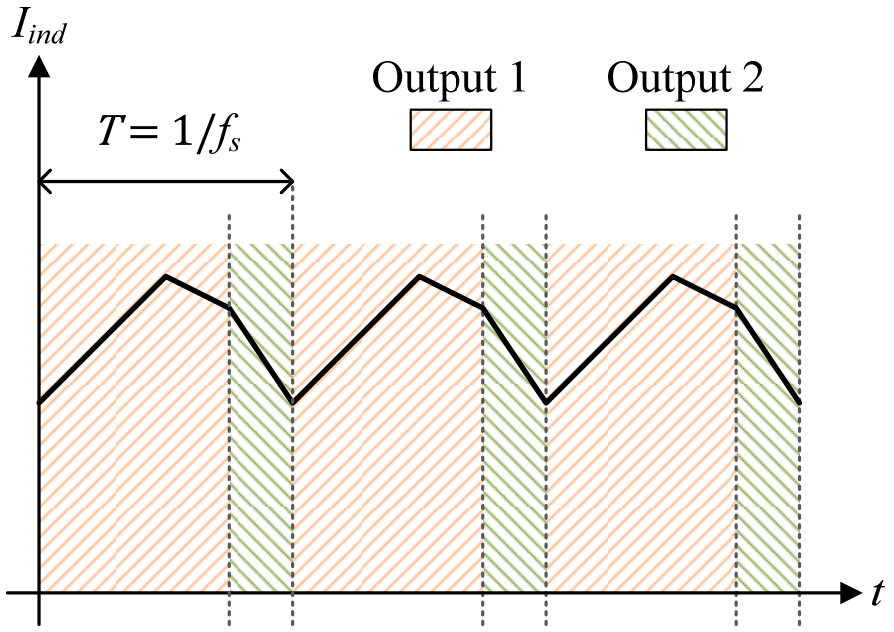


Figure 2.2. Typical timing diagram of the inductor current for dual-output buck converters.

shown in Fig. 2.3. However, when the number of outputs gets larger, instability occurs in many regions of operation if plain nested PWM loops are used. The same group presented an improved scheme to solve the unstable issue by suitably combining the errors from each output before driving the nested PWM generators as shown in Figs. 2.4 and 2.5 [13], [42]. The equations used to linearly combine the errors for a 4-output case are:

$$\begin{aligned} X_1 &= \varepsilon_1 + \varepsilon_2 + \varepsilon_3 + \varepsilon_4 \\ X_2 &= \varepsilon_1 - \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\ X_3 &= \varepsilon_1 + \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\ X_4 &= \varepsilon_1 + \varepsilon_2 + \varepsilon_3 - \varepsilon_4 \end{aligned} \tag{2.1}$$

This work successfully regulates each output independently with a good stability. However, the error combination circuits are relatively complicated and power hungry. Besides, since each

output is PWM controlled, the bandwidth is usually ten times slower than the switching frequency. Hence, this topology suffers from slow transient response and poor cross-regulation. It usually also requires larger off-chip output capacitors compared to the single-output topology to mitigate the overshoot/undershoot due to the nature of time multiplexing and slow switching.

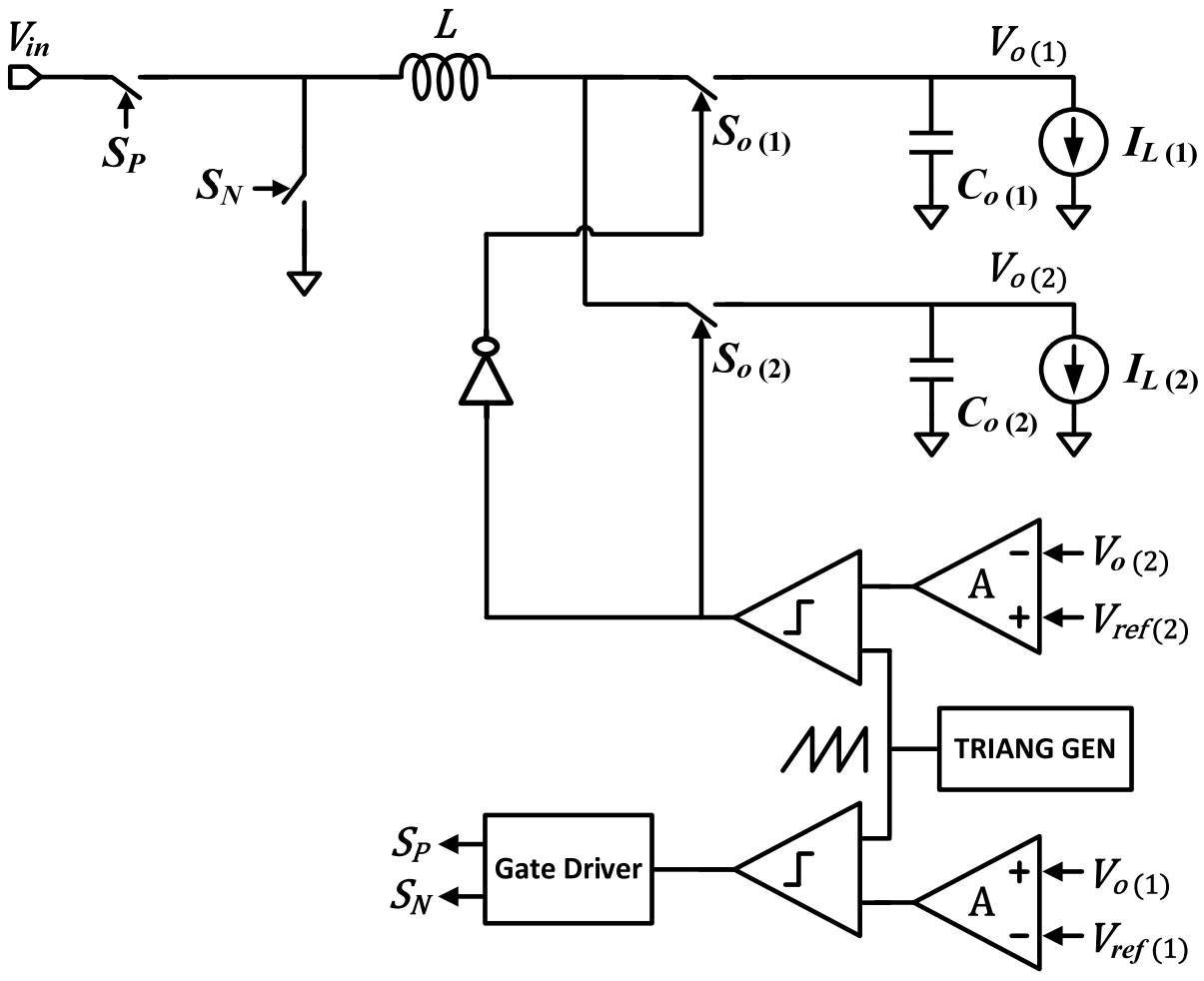


Figure 2.3. Block diagram of the single-inductor dual-output buck converter with nested PWM control in [12].

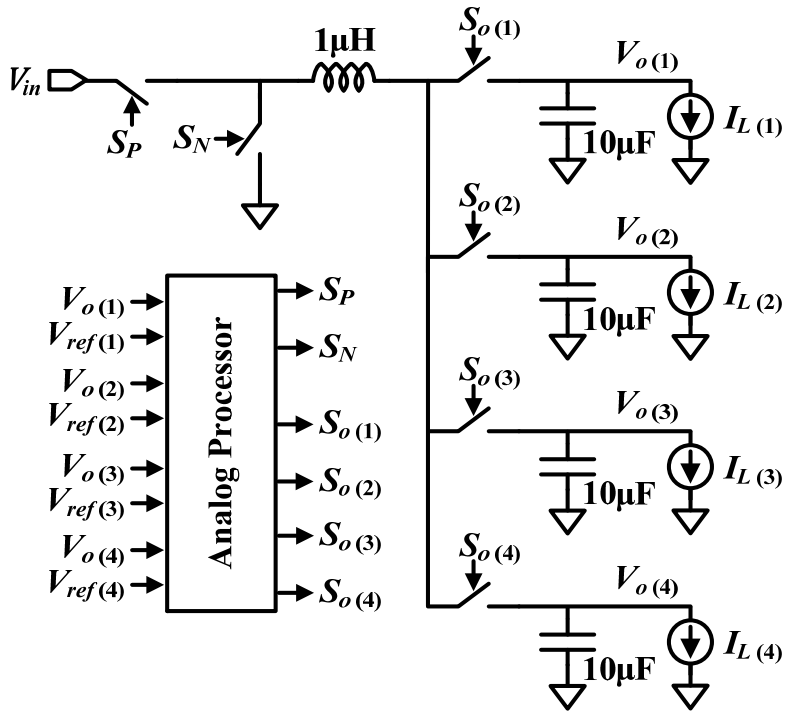


Figure 2.4. Block diagram of the single-inductor 4-output buck converter with nested PWM control in [13].

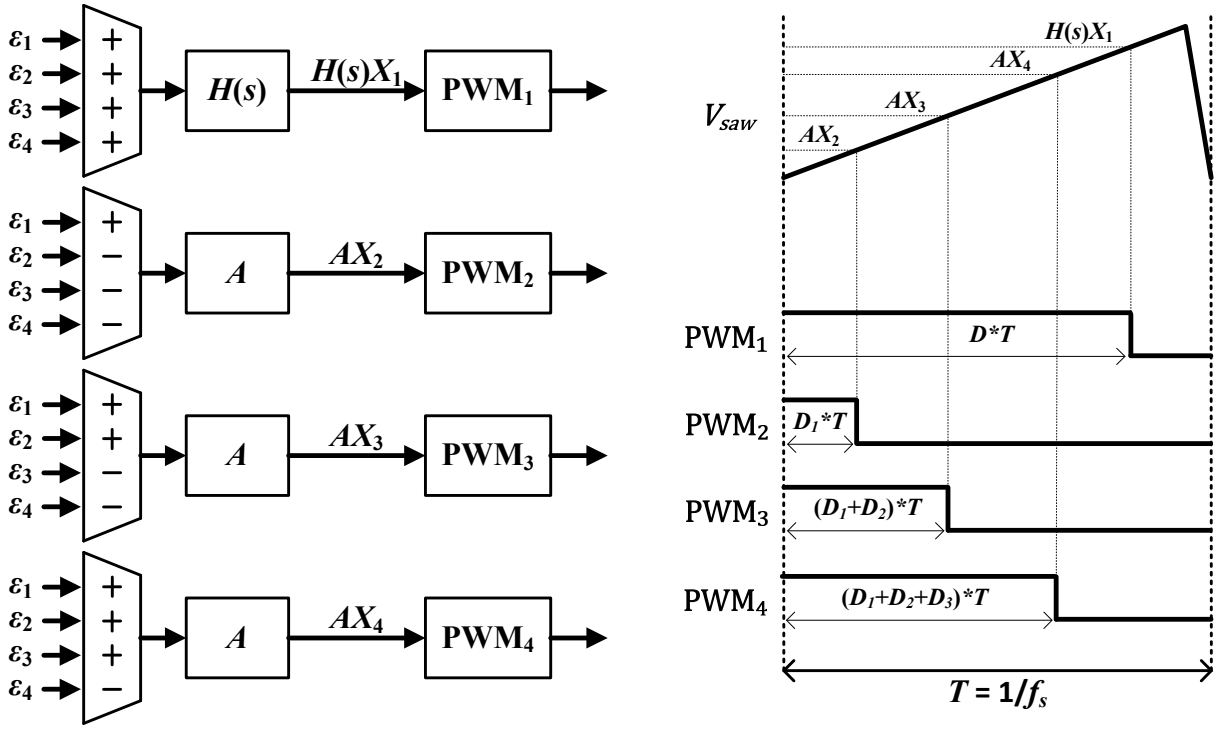


Figure 2.5. Conceptual scheme of the analog processor and nested PWM outputs in [13].

2.2 PLL-Based Bang-Bang Control SIMO Buck Converters

In addition to slow transient response, using nested PWM generators requires multiple Proportional-Integral (P-I) compensators which inevitably increases the design complexity and chip area. The work in [14] presents an ordered power-distributive control for a 5-output boost converter as shown in Fig. 2.6. In this design, comparator-based control is applied to the first four outputs and all errors of these outputs are transferred and accumulated to the last one which is then regulated by a single PWM generator. Therefore, the first four outputs can respond load transients quickly and only the last output requires a compensation network in the feedback loop which greatly reduces the overall cost. However, the last output continues suffering from slow transient response and serious cross-coupling still appears on every output.

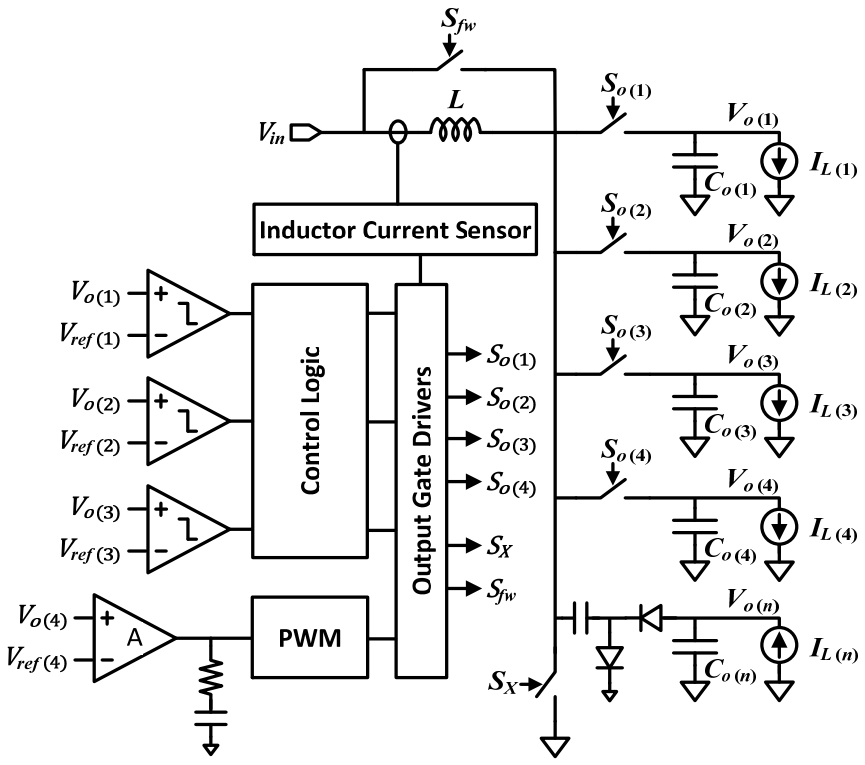


Figure 2.6. Block diagram of the single-inductor 5-output boost converter with ordered power-distributive control in [14].

Thus, the work in [15] is modified from the ordered power-distributive control and presents a 6-output buck converter as shown in Fig. 2.7. The first five outputs are still regulated by comparators but a PLL-based bang-bang controller is applied on the last output instead of a PWM generator. The bang-bang control switching converter is very easy to implement and extremely fast on responding any load transients. Unlike current/voltage-mode PWM control, compensator is not needed because bang-bang control converters are stable irrespective of their load condition [20]. Unfortunately, the switching frequency is not constant and it is problematic to design an EMI filter if the load is a noise-sensitive circuit. Therefore, by adding a PLL loop within the bang-bang control can maintain a constant switching frequency and keep all the merits of the original bang-bang control.

In this topology, the output power distribution switches are turned on one by one in descending order of priority and all the errors of the first five outputs are transferred to the last output voltage like [14]. However, the voltage ripple on the last output is out of phase with the inductor current ripple due to time multiplexing and the order of energy transfer, this signal can not be used directly to the bang-bang controller. Therefore, the average error signal from all outputs is used to make the in-phase voltage ripple and then combined with the inductor current signal together feeding into the hysteresis comparator to generate the switching frequency. The phase difference between the reference frequency and the switching frequency is converted to a control signal V_c that is used by the VCO. As illustrated in Fig. 2.8, the converter itself actually behaves like this VCO in the PLL loop. The main feature of this PLL-based bang-bang control comparing with PWM control is that it is free from stability issue and achieves fast and accurate load and line-regulation.

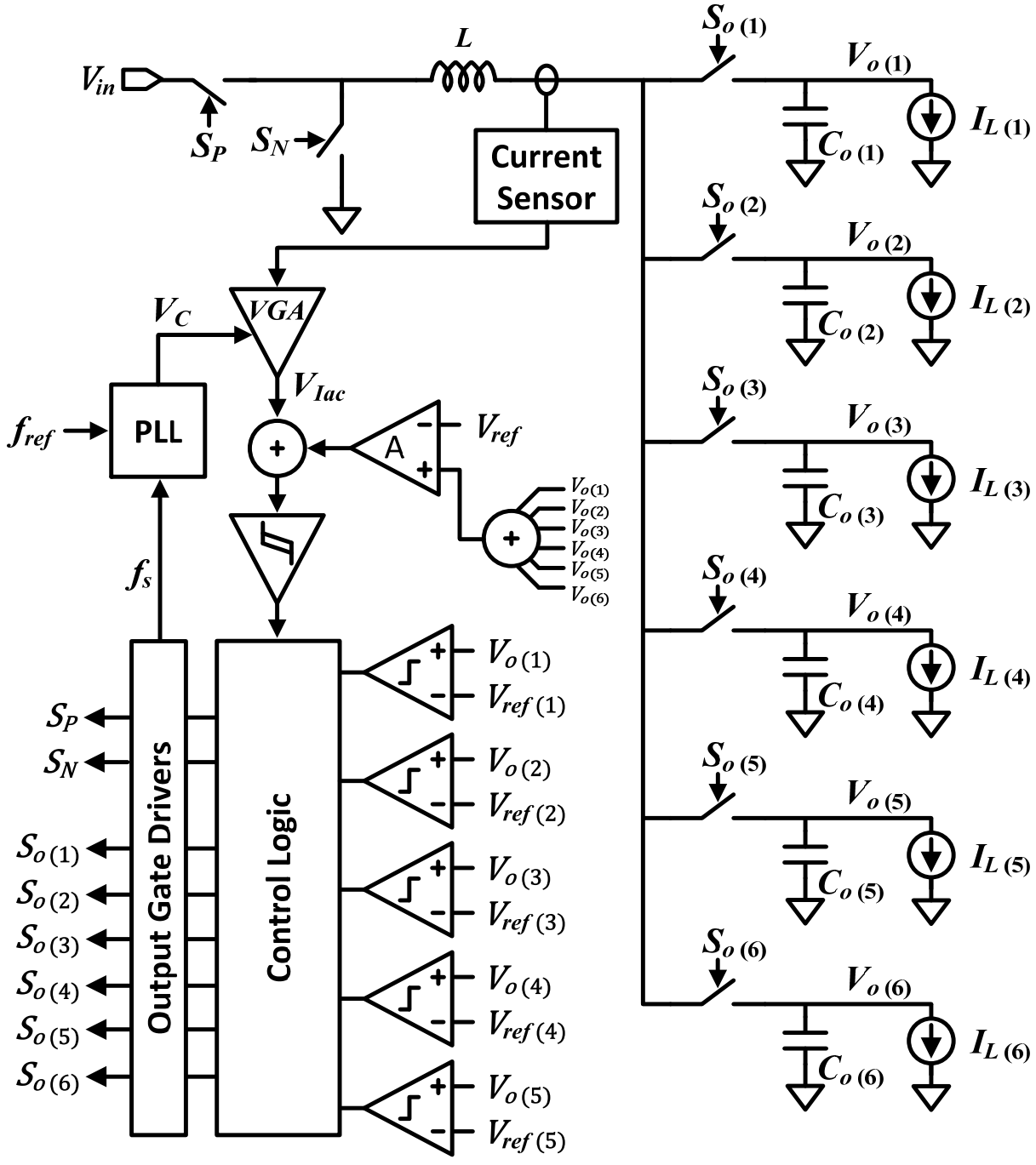
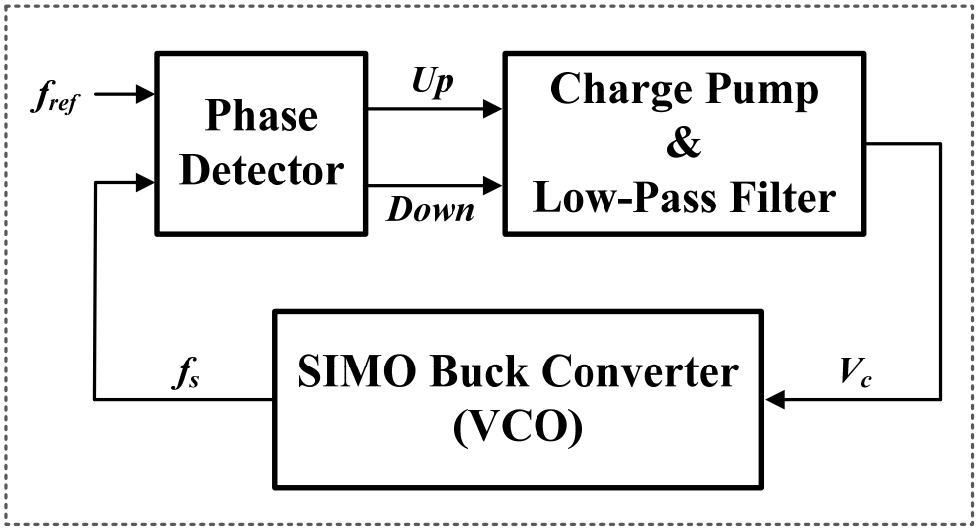


Figure 2.7. Block diagram of the single-inductor 6-output buck converter with PLL-based bang-bang control in [15].



PLL Control Loop

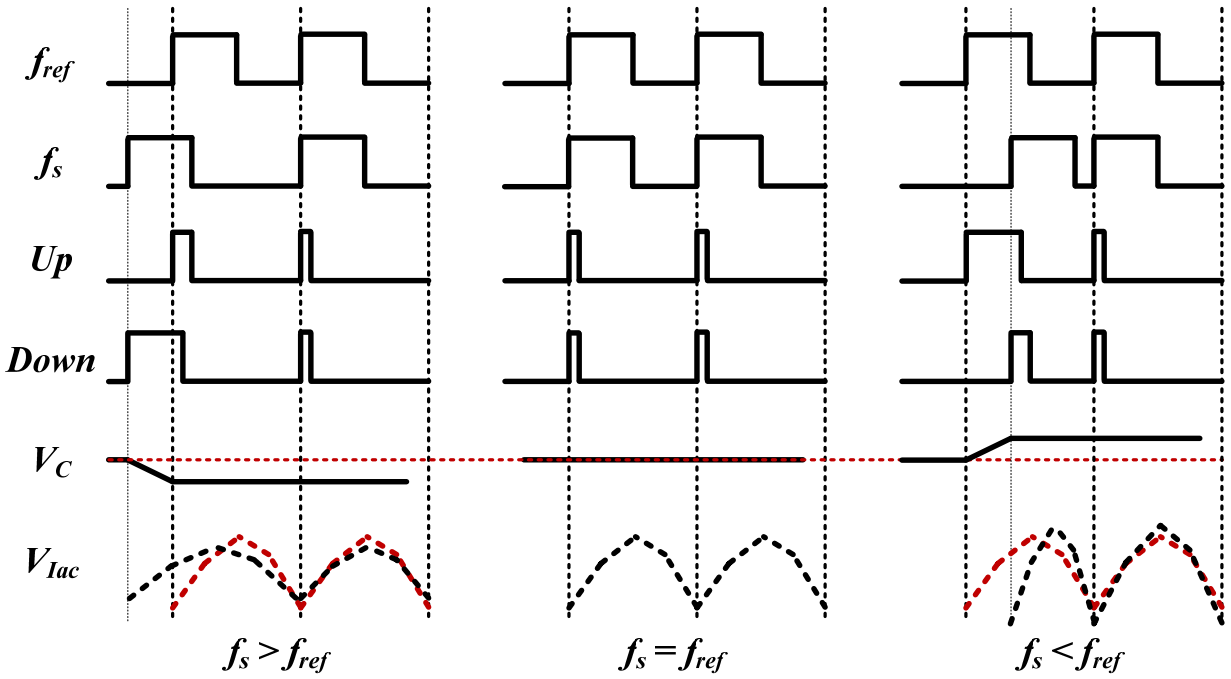


Figure 2.8. Operation principle of the PLL-based bang-bang control in [15].

2.3 Freewheeling Current/Duty Control SIMO Buck Converters

A pseudo-continuous conduction mode SIMO boost converter with freewheel switching is first presented in [22]. The idea to add a freewheeling period is to keep the converter operating in Discontinuous Conduction Mode (DCM) even at heavy load condition. By doing this, cross-coupling and stability issue between each output can be solved. The freewheeling switch is an extra switch connecting the two terminals of the inductor. When it is turned on, i.e. freewheeling period, the inductor current is freewheeled inside the loop formed by the switch and the inductor without any loss ideally. However, since Equivalent Series Resistance (ESR) of the inductor and the on-resistance of the switch, a small amount of energy is lost in real implementation. Fig. 2.9 shows the power stage of a SIMO boost converter with the freewheeling switch.

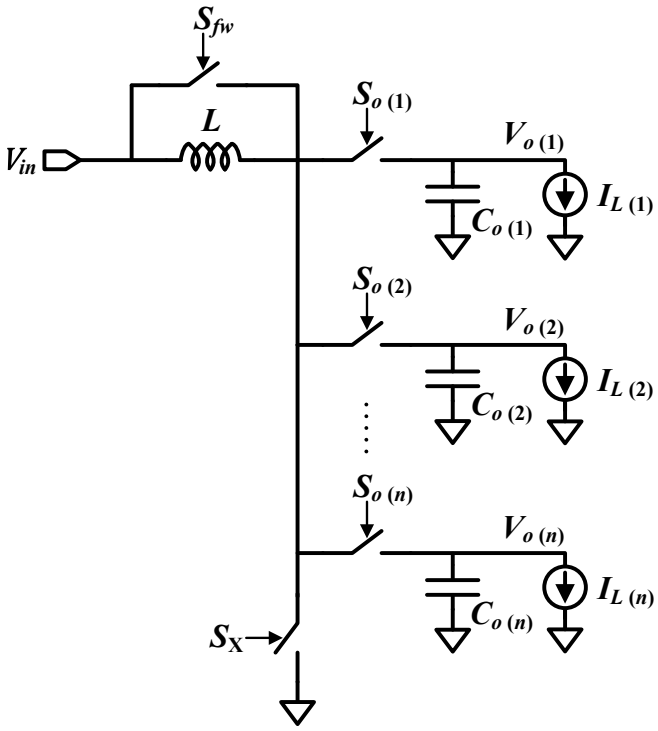


Figure 2.9. Power stage of the SIMO boost converter with freewheeling switch presented in [22].

The work in [16] utilizes this freewheeling switch and presents a freewheeling current control SIMO boost converter as shown in Fig. 2.10. This control scheme is also modified from the ordered power-distributive control [14] mentioned in section 2.2. In the ordered power-distributive control, the last output is PWM controlled with an error amplifier in the feedback loop. It implies that the last output loading condition continuously affects the control loop. This is an undesirable characteristic for stability consideration. Therefore, the main feedback loop of the converter needs a new control variable other than output voltages in order to exclude the output pole composed of the output filtering capacitor and equivalent load resistor. The freewheeling current control chooses the reserved inductor current during the freewheeling period as the control variable for the main loop. Since all the outputs are comparator-based control, the errors of the outputs will be accumulated and shown on the freewheeling current. By regulating the freewheeling current to a reference with peak current-mode control, the main control loop will charge either more or less energy in the inductor corresponding to the output loads without sensing the output nodes directly. Thus, this control scheme is frequency independent on the values of the inductor, output capacitor and load equivalent resistor. The loop compensator can be greatly simplified and the output response can be as fast as a hysteresis converter. The operational timing diagram of a boost converter with freewheeling current control is shown in Fig. 2.11, where single-output is used for simplicity. The left side of Fig. 2.11 shows an operation in the light load condition, where the freewheeling current level is low but the period is long. In contrast to the heavy load condition on the right side, the freewheeling current level is high but the period is short. However, the average freewheeling current ($D_{fw} \times I_b$) in steady-state for both cases should be the same and equal to the reference (I_{fw_ref}) in this control scheme.

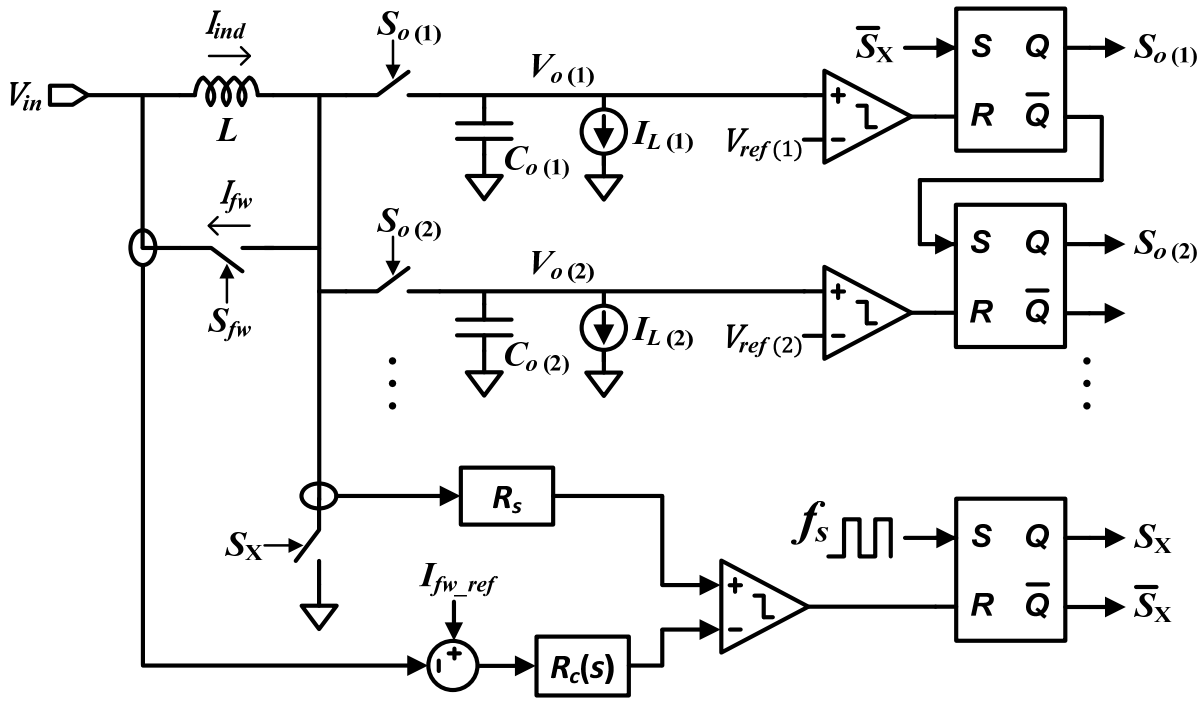


Figure 2.10. Block diagram of the SIMO boost converter with freewheeling current control in [16].

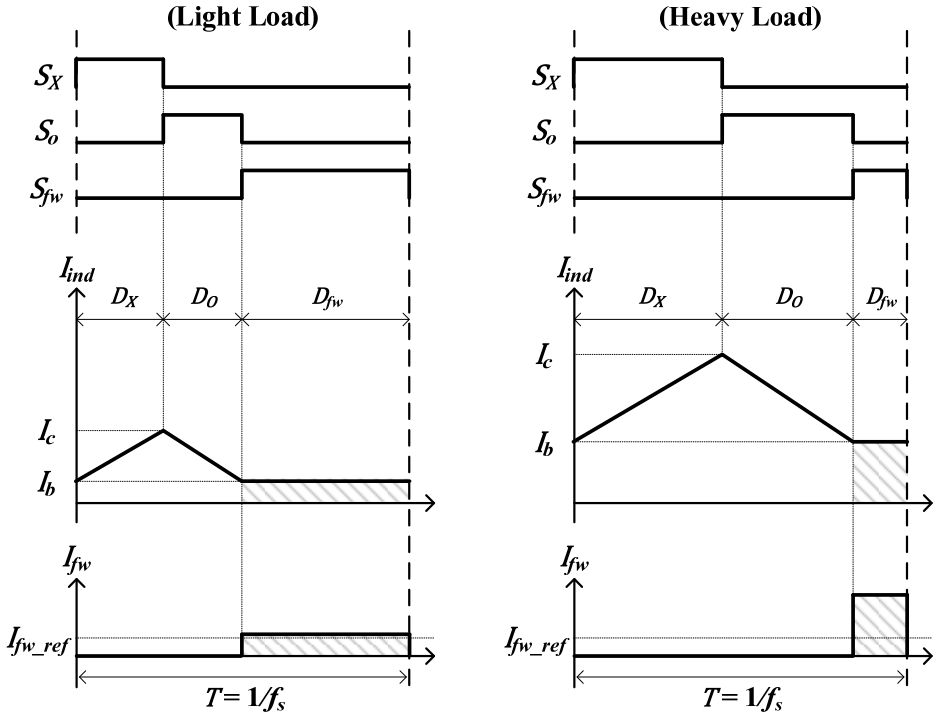


Figure 2.11. Operational timing diagram of a single-output boost converter with freewheeling current control in [16].

Similar idea is used in [17] to implement a SIMO buck converter with some modifications as shown in Fig. 2.12. First, instead of regulating the freewheeling current, the duty cycle of the freewheeling period is controlled by a reference which can be adaptively adjusted according to the output loading condition. Higher load currents lead to a shorter duty to minimize the conduction loss. This duty behaves like a buffer region if any load transient happens. Second, a charge control is used for ordered power distribution to each output instead of the comparator-based control. The charge control has the advantage of accurately regulating the average current through a switch per cycle, and therefore the energy delivered to each output can be well controlled [23]. Third, the freewheeling switch is connected between the node V_{LXP} and the battery instead of the two terminals of the inductor. In fact, the freewheeling switch can also be connected between V_{LXP} and the ground. These three different connections are design options that can be chosen depending on the real implementation. Fig. 2.13 shows detailed block diagram of the control circuit. The phase difference between S_{fw} and S_{fw_ref} is detected and converted to an error signal ($V_{c\,(6)}$) used by the peak current-mode control for the main loop to generate the on/off duty of the input switches (S_P and S_N). The main loop should be designed slower than the local loops for the outputs. The pulse-skipping function for each output is also allowed for Pulse Frequency Modulation (PFM) mode operation. This implementation demonstrates good output load and cross regulations, but the transient response is slow due to limited loop bandwidth.

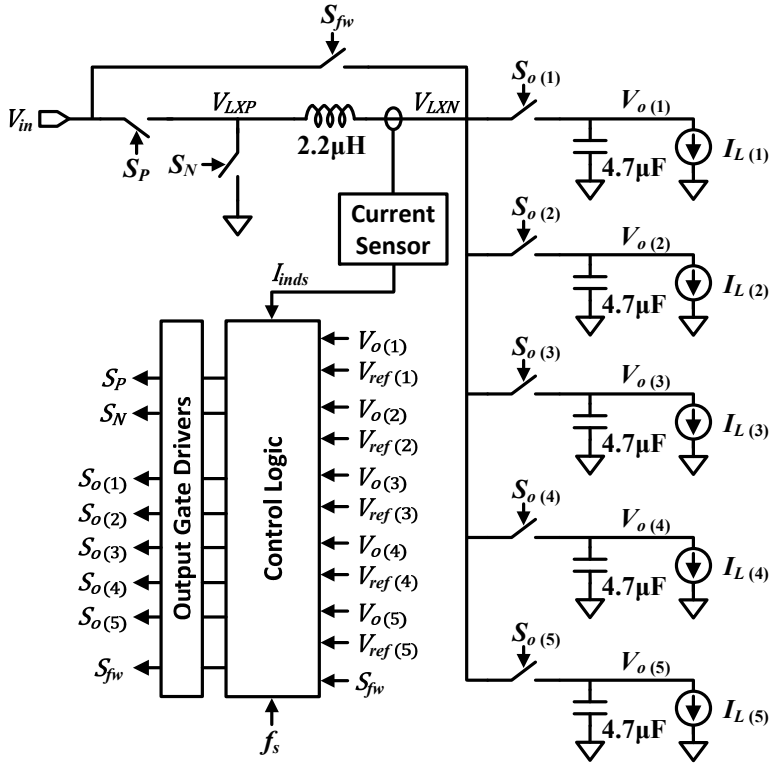


Figure 2.12. Block diagram of the SIMO buck converter with freewheeling duty control in [17].

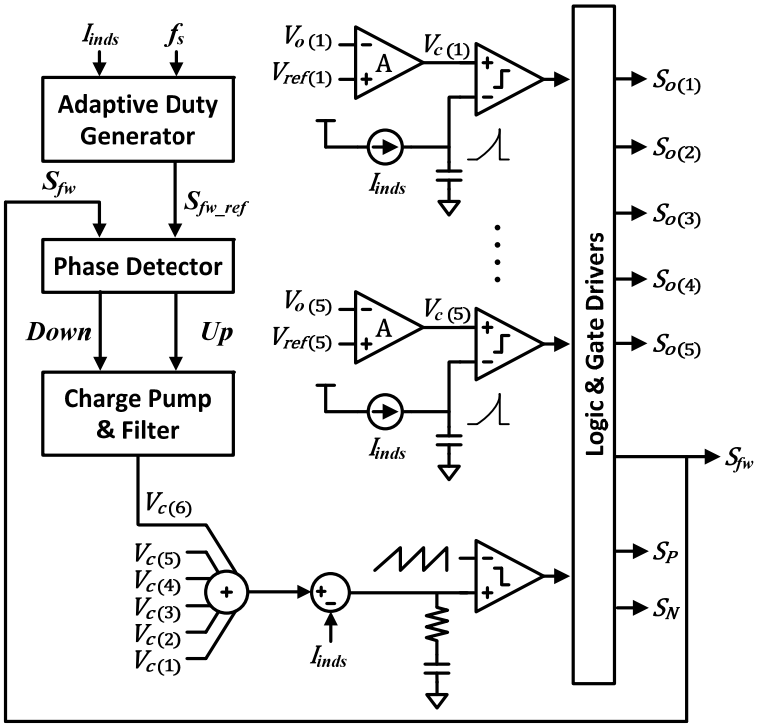


Figure 2.13. Block diagram of the control circuit in [17].

2.4 Adaptive Off-Time Control SIMO Buck Converters

In order to enhance the system power efficiency, DVS technique is widely used in single-output converters by providing variable voltage with fast reference tracking. However, serious cross coupling and slow transient response of the SIMO converters usually limit the application of this technique. Although freewheeling current or duty control enables SIMO converters regulating all the outputs by comparators to achieve better cross-regulation and faster transient response, the extra switching and conduction losses from the freewheeling switch tradeoff its advantages. The work in [18] presents a ripple-based adaptive off-time control SIMO buck converter which improves the cross-regulation on each output and realizes fast load/reference transient responses without any efficiency degradation.

Fig. 2.14 shows the architecture of a 4-output buck converter with this off-time control. Unlike conventional comparator-based control, all the outputs are regulated by comparators to time-share the energy stored in the single inductor without any extra switch (e.g. freewheeling switch). The switching frequency is locked to the reference clock with an adaptive off-time generated by the PLL unit. This off-time determines the duty of the input power generation switches (M_P, M_N). As the inductor current ramps up and down, the output power distribution switches ($M_{o\,(1)} - M_{o\,(4)}$) are turned on one by one according to the output states of the corresponding comparators. The power switch M_P is turned off when $M_{o\,(1)}$ is turned on to charge the first output $V_{o\,(1)}$. When the off-time period is expired, M_P is turned on and M_N is turned off to increase the inductor current until $V_{o\,(4)}$ is higher than its reference $V_{ref\,(4)}$ and $V_{o\,(1)}$ is being charged again. The steady-state can be reached for any line/load condition by adjusting the off-time length.

Since the bandwidth of the PLL is usually less than one-tenth of the reference clock, the off-time can be considered as a fixed value in the beginning of the load and reference transition. Hence the switching frequency has to be changed during the transient response to immediately react to the load demand. However, it is locked in steady-state to avoid the unpredictable noise spectrum from switching. Furthermore, due to the charge error of all the outputs is accumulated and cancelled by adjusting the switching frequency instead of the freewheeling period, this control scheme can achieve a good cross-regulation performance without sacrificing the efficiency. The block diagram of the adaptive off-time control loop is shown in Fig. 2.15.

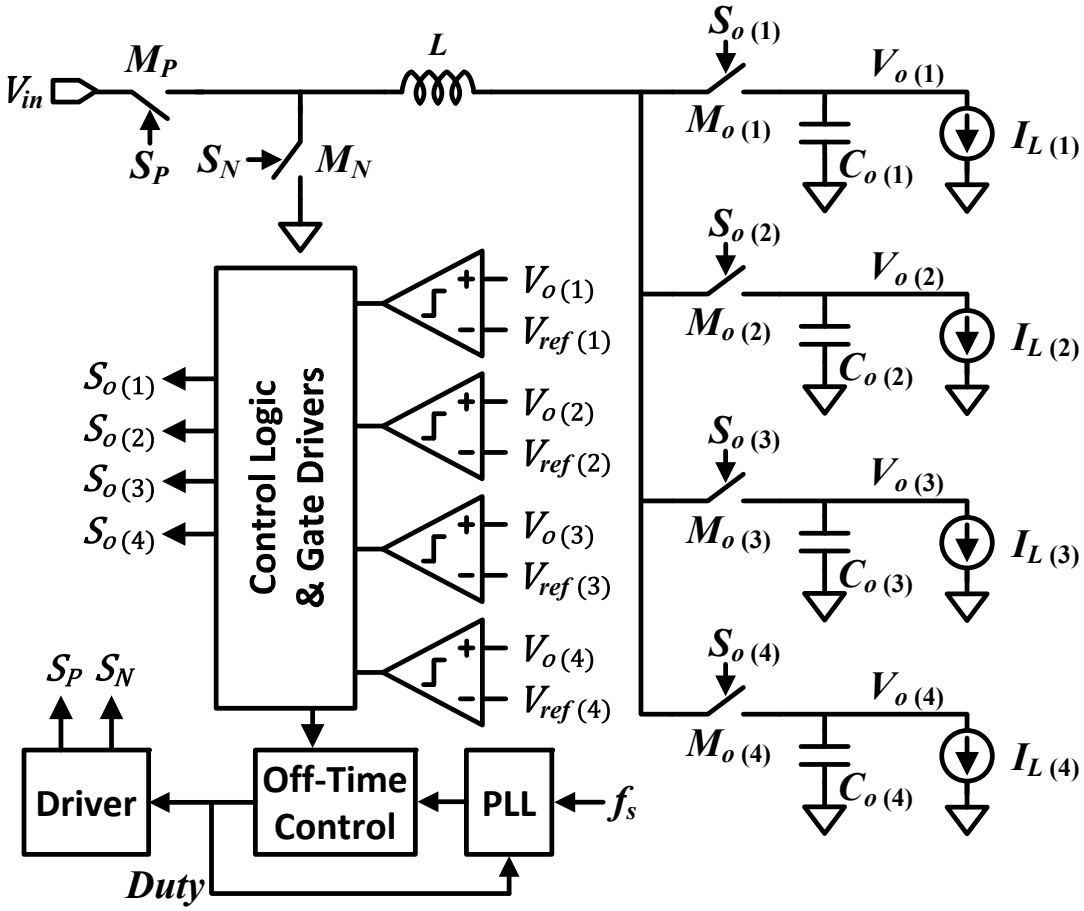


Figure 2.14. Block diagram of the SIMO buck converter with adaptive off-time control in [18].

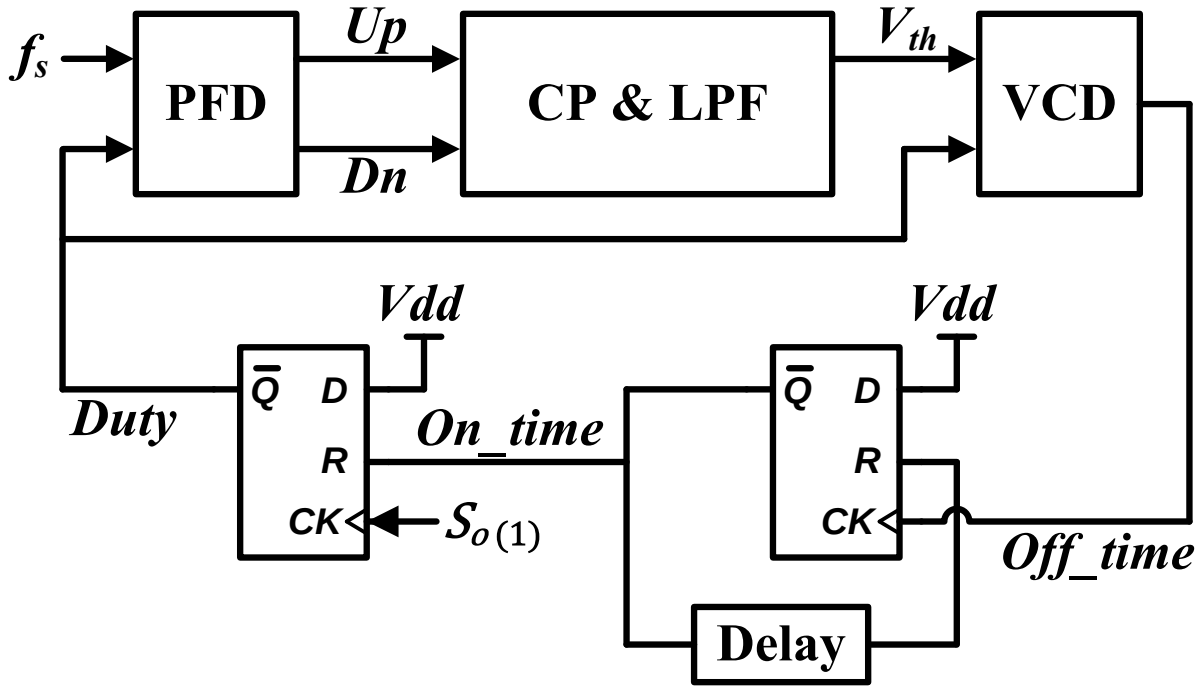


Figure 2.15. Block diagram of the adaptive off-time control in [18].

2.5 Conclusion

Conventional SIMO converters serve as good candidates to generate multiple outputs with a single off-chip inductor. Several previous arts have been presented to improve the load- and cross-regulation performance as well as dynamic response. However, these converters typically operate at 0.5–2 MHz to maintain high efficiency. Thus their bandwidths continue being limited by the switching frequencies. A strategy to increase the bandwidth may be to switch the entire converter at much higher frequencies, similar to many reported single-output high-frequency switching converter implementations. But this strategy erodes the high power conversion efficiency advantage of SIMO converters. Therefore, efficiency, cost and dynamic performance trade off each other fundamentally for all the conventional solutions.

CHAPTER 3

PROPOSED DF-SIMO TOPOLOGY

In order to make SIMO architectures more attractive for SoC applications, we must resolve the issues of large passive components, large number of package pins, poor cross- and load-regulation, and slow dynamic response. Since the target application is SoCs, which are typically implemented in nanometer CMOS node, the very high speed-to-power ratio of these technologies (65 nm and beyond) can be leveraged to alleviate these limitations while maintaining high power conversion efficiency. To that effect, I propose the Dual-Frequency SIMO (DF-SIMO) architecture with freewheeling current control. Two switching frequencies are applied on the converters instead of conventional single switching frequency. This novel topology introduces another design parameter (i.e. output switching frequency) to improve the dynamic performance without causing excessive switching loss. The detail operation principle, tradeoffs and advantages are explained and discussed in section 3.1 and 3.2.

3.1 Operation Principle of the DF-SIMO Topology

The proposed DF-SIMO topology is depicted in Fig. 3.1 [24], [25]. It is similar to conventional SIMO topologies [12]–[20] except that the output stage distributes power to the outputs at a much higher rate (f_o) than the switching rate of the input stage (f_{in}). Thus, within a single input switching period ($T_{in} = 1/f_{in}$), each output is served multiple times (once every output switching period ($T_o = 1/f_o$)) as shown in Fig. 3.2, where a ratio of 4 between f_o and f_{in}

and only 2 outputs are used for simplicity. By making f_o sufficiently high (>100 MHz), the output capacitors can be scaled to on-chip levels, and by keeping f_{in} sufficiently low (~2 MHz) and continuing to use an off-chip inductor, low switching losses in the input stage and its simple design can be preserved. Each output ($V_{o(i)}$) is regulated using a high-speed comparator that detects when the output exceeds its reference ($V_{ref(i)}$), and turns the corresponding power switch ($M_{o(i)}$) off, and turns on the switch ($M_{o(i+1)}$) corresponding to the next output ($V_{o(i+1)}$). If the inductor current (I_{ind}) is constant and equal to the sum of all the loads ($\sum_i I_{L(i)}$), this sequence repeats every T_o, which produces a steady-state local duty-cycle ($dc_{o(i)} = T_{on(i)}/T_o$) for each output such that $I_{L(i)} = \left(dc_{o(i)} \times I_{ind}\right)$.

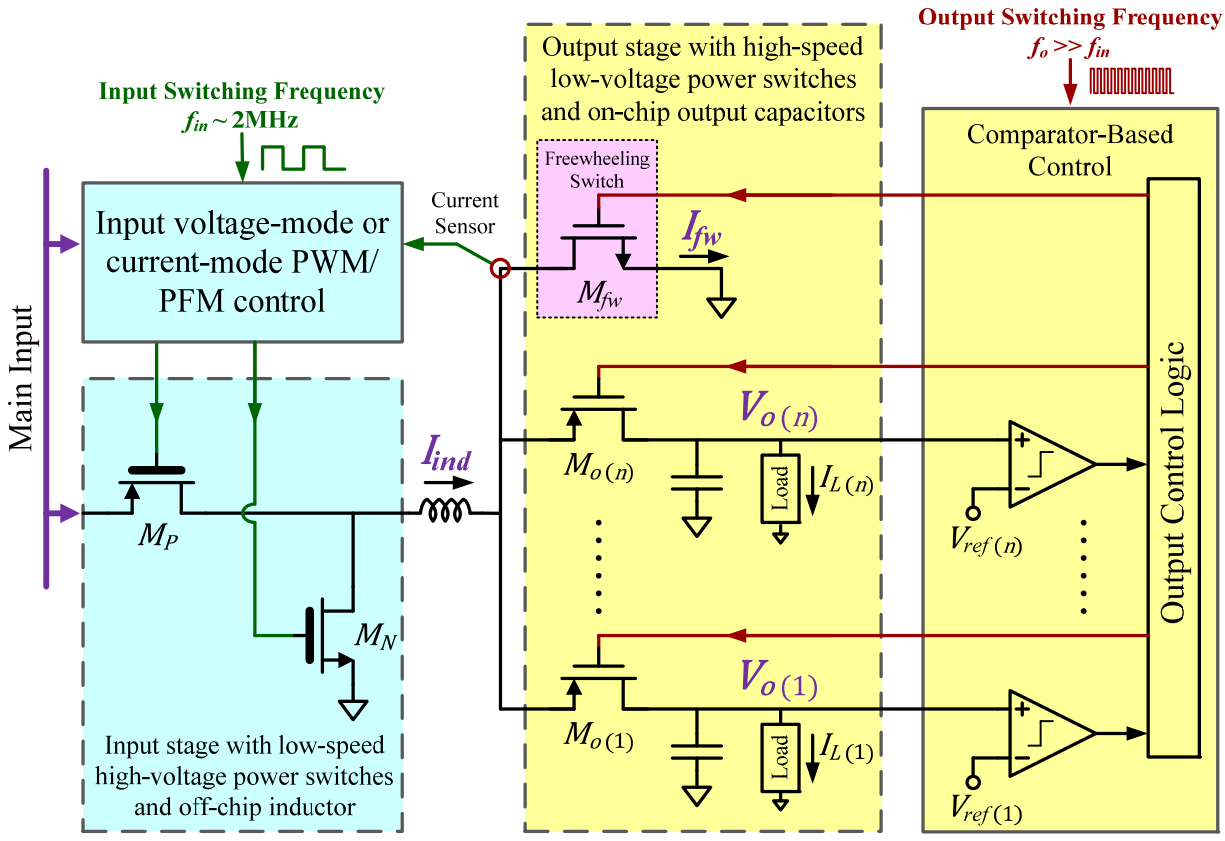


Figure 3.1. Block diagram of the proposed DF-SIMO topology.

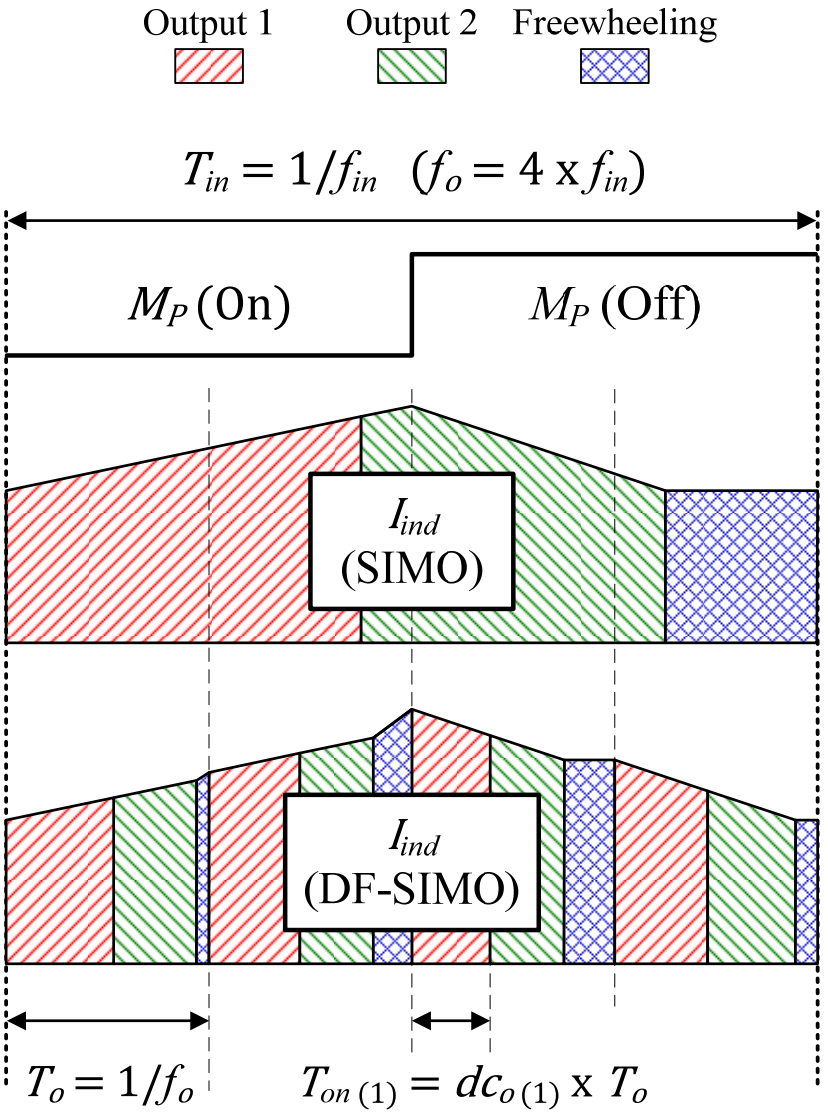


Figure 3.2. The inductor current distribution process to the outputs assuming only two outputs and an output switching frequency of 4 times the input switching frequency.

However, the output control scheme described above suffers from two major issues that must be addressed. First, since the inductor current contains a low-frequency ripple component due to the input stage switching at f_{in}, the aforementioned steady-state will be continuously disturbed, and the local duty-cycle of each output will change every output switching period such

that $I_{L(i)} = \left(dc_{o(i)} \times I_{ind}\right)$ is maintained regardless of the actual value of I_{ind}. As the inductor current rises above its average, the local duty-cycles of the outputs drop, thus leaving the final output with the burden of absorbing whatever energy is left in the inductor regardless of its own load demand. Moreover, as the inductor current drops below its average, the duty-cycles of the outputs rise, thus depriving the final output from the energy needed to sustain its own load. This mechanism implies that it is impossible to continue to use comparator-based control for the final output, and an alternative Pulse Width Modulation (PWM) scheme must be used instead at the expense of large low-frequency voltage ripples at the final output due to its small on-chip capacitor as shown in Fig. 3.3.

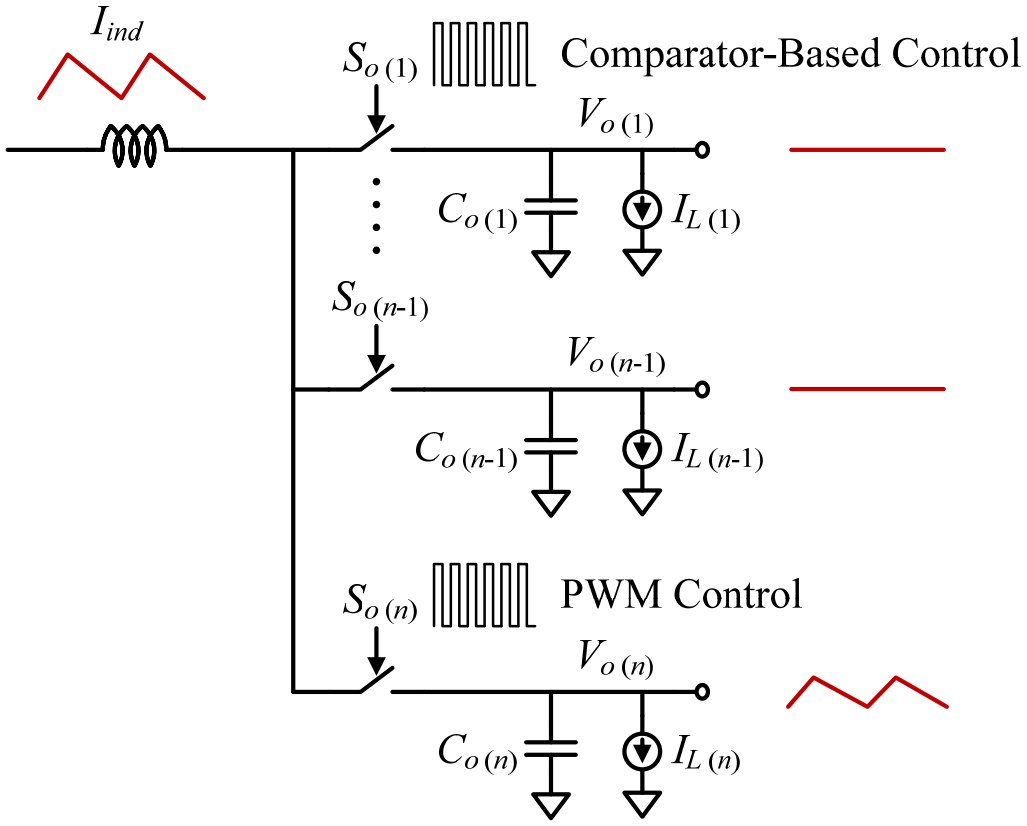


Figure 3.3. Large low-frequency voltage ripples at the final output if the PWM control is used.

Although an off-chip capacitor at the final output only may be used to reduce this low-frequency voltage ripple, the high output switching frequency combined with the package parasitics of the chip and the external capacitor would result in high-frequency glitches that far exceed in magnitude the low-frequency voltage ripple. Second, since the inductor current is distributed to the outputs at a high rate, fast output dynamic behavior should be expected in response to load or output voltage changes. However, since the energy stored in the inductor can only change as fast as the input switching frequency, the dynamic response of the outputs continues to be limited by that frequency. This results in large undershoots and overshoots, long settling time, and poor cross regulation as the outputs compete for the inductor energy, all of which offset the benefit of the high output switching frequency in terms of dynamic response.

To resolve these two issues, a freewheeling switch (M_{fw}) in the output stage is employed, but unlike conventional SIMO topologies [12]–[20], the DF-SIMO operates it at the same high frequency as the rest of the output switches [24], [25] by turning it on once every output switching period after all the outputs have been served. The freewheeling switch serves three purposes: (a) bears the burden of absorbing the steady-state low-frequency inductor current ripple so that the final output can be regulated by comparator-based control with only an on-chip capacitor; (b) provides a collective error signal to control the input stage; and (c) provides a mean to efficiently ensure a reserve of energy in the inductor to aid with the output dynamic response.

To accomplish (a), the valley of the inductor current in steady-state must be at least equal to the sum of all the load currents so as to ensure that the inductor has enough energy to serve all the outputs within any output switching period. This condition implies that the inductor current ripple would always result in excess charge, which is absorbed by the freewheeling switch, i.e.

its local duty-cycle (dc_{fw}) is always higher than zero. It also implies that the inductor always operates in Continuous Conduction Mode (CCM). Considering that the average inductor current (I_{ind_avg}) is equal to the average freewheeling current (I_{fw_avg}) plus the sum of all the loads, I_{fw_avg} must therefore be regulated to be larger than approximately half the inductor current ripple (ΔI_{ind}) as illustrated in Fig. 3.4. This can be accomplished by using a freewheeling current control scheme [16], where I_{fw_avg} is regulated to a reference level (I_{fw_ref}) using a low-frequency PWM loop that controls the input stage. Therefore, by using the average freewheeling current to control the input stage and setting I_{fw_ref} to be larger than ($\Delta I_{ind}/2$) [24], [25], both purposes (a) and (b) are satisfied.

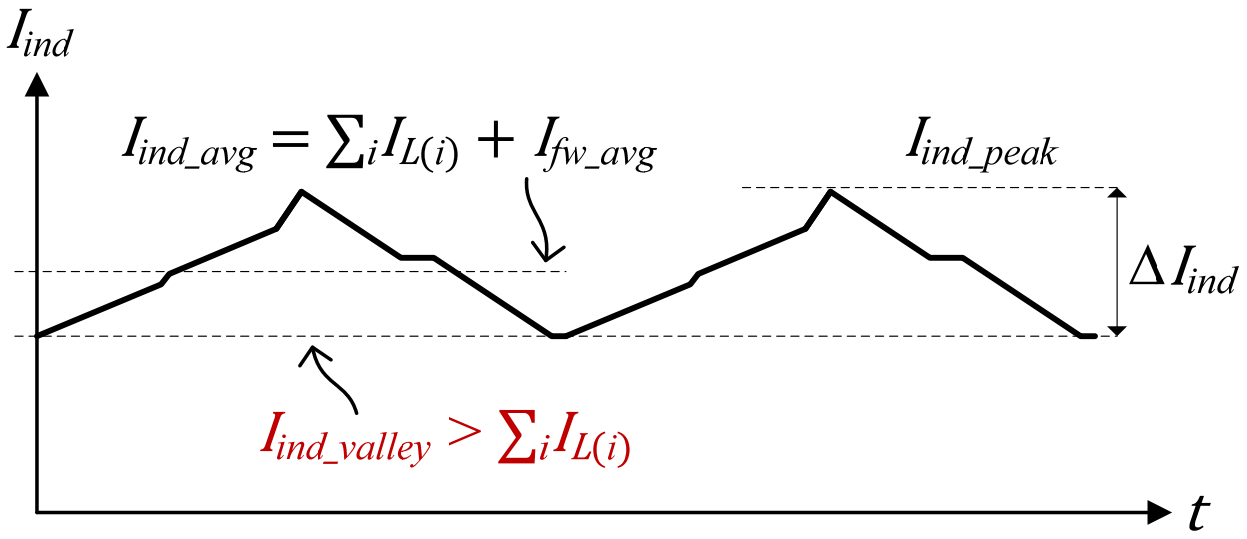


Figure 3.4. Steady-state inductor current profile of the proposed DF-SIMO topology.

The freewheeling switch configuration with M_{fw} switching at the same high rate as the rest of the outputs accomplished purpose (c) in two ways. First, it provides an efficient escape

route for the inductor's excess current every output switching period in case the loads suddenly drop. Second, it guarantees an efficient reserve of current in the inductor, which can be routed to the outputs every output switching period in case their loads suddenly increase. This results in an output dynamic response that is as fast as the output switching frequency without waiting for the slow input stage to adapt. It also ensures better cross regulation as each output is refreshed every output switching period. However, it is worth noting that the number of output switching periods needed for the outputs to settle after a load step is a function of the energy reserve in the inductor. Thus, increasing I_{fw_avg} yields better dynamic response and cross-regulation performance. Moreover, cross-regulation can be further improved by output-reordering based on load changes, which will be discussed in further details in chapter 5.

3.2 Tradeoffs and Advantages of the DF-SIMO Topology

In order to properly implement the DF-SIMO topology, several metrics and tradeoffs must be considered. This includes the choice of the output switching frequency and capacitors for a given voltage ripple and the choice of the freewheeling current.

3.2.1 Output Switching Frequency, Output Capacitors, and Voltage Ripple Tradeoffs

As all the outputs are regulated every output switching period using comparator-based control, the steady-state voltage ripple ($\Delta V_{o(i)}$) associated with the i^{th} output shown in Fig. 3.5 can be written as [25]:

$$\Delta V_{o(i)} = \frac{\left(I_{ind} - I_{L(i)}\right) \times dc_{o(i)}}{f_o \times C_{o(i)}} = \frac{\left(1 - \frac{I_{L(i)}}{I_{ind}}\right) \times I_{L(i)}}{f_o \times C_{o(i)}} \tag{3.1}$$

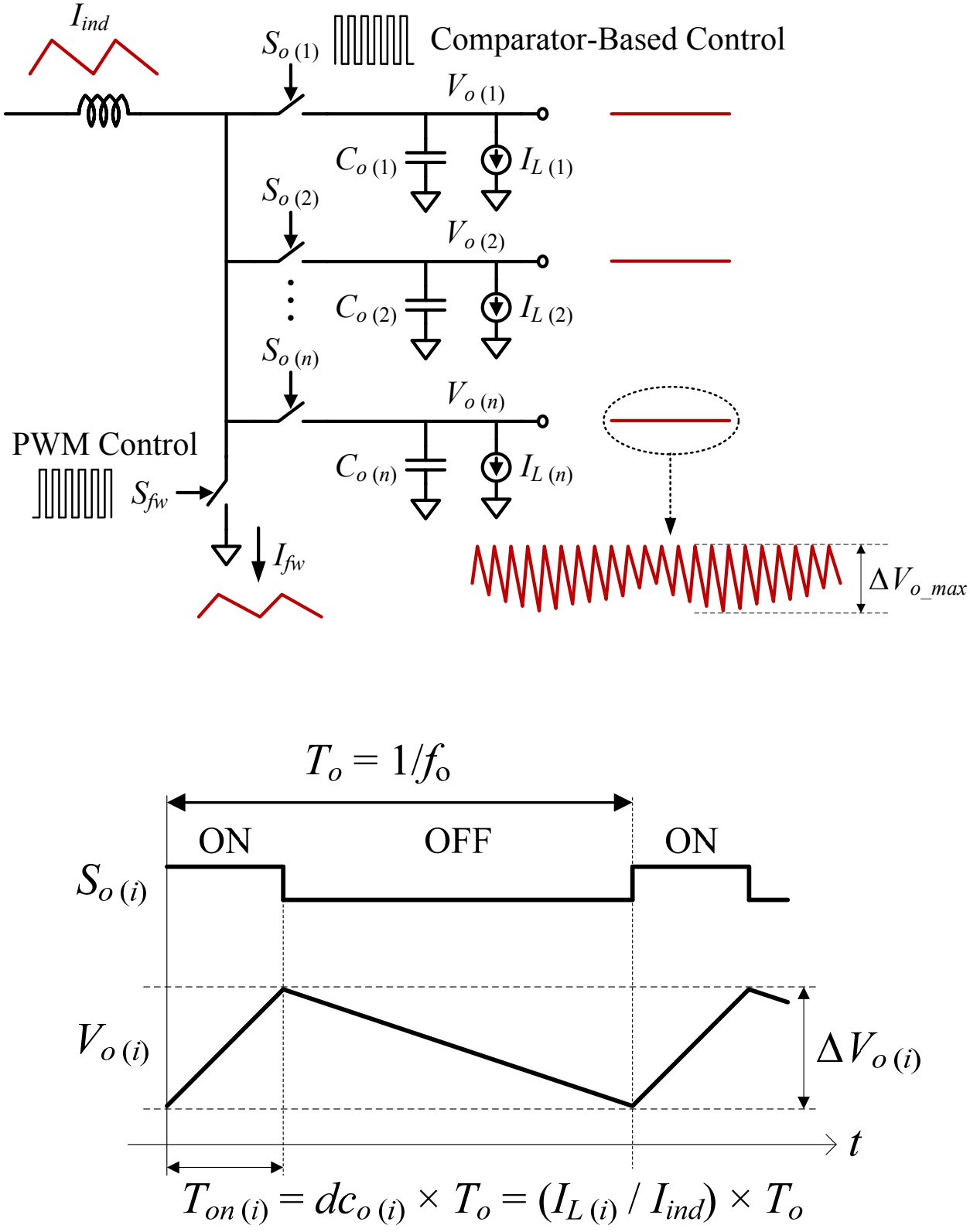


Figure 3.5. Steady-state output voltage ripple of the proposed DF-SIMO topology.

where ($C_{o(i)}$) is the output capacitance at the i^{th} output, and all the other parameters are defined in the previous section. Eq. (3.1) implies that $\Delta V_{o(i)}$ varies with the inductor current, and thus, the voltage ripple magnitude tracks the low-frequency inductor current ripple, and its maximum occurs at the peak inductor current (I_{ind_peak}) and the maximum load current ($I_{L\_max(i)}$) as follows:

$$\Delta V_{o\_max(i)} = \frac{\left(1 - \frac{I_{L\_max(i)}}{I_{ind\_peak}}\right) \times I_{L\_max(i)}}{f_o \times C_{o(i)}} \tag{3.2}$$

Eq. (3.2) suggests a tradeoff between the maximum voltage ripple at a given output versus the capacitor size and the maximum load of that output, the inductor peak current, and the output switching frequency. For instance, if a given output has a maximum load of 20 mA and an output capacitance of 2 nF, and assuming an inductor peak current of 100 mA and an output switching frequency of 100 MHz, the maximum voltage ripple at that output would be 80 mV. If this voltage ripple needs to be reduced, then the maximum load current of this output must be reduced, or alternatively, either the output switching frequency or the output capacitance must be increased at the expense of higher switching losses or larger silicon area.

3.2.2 Freewheeling Current Tradeoffs

As discussed in section 3.1, to ensure proper steady-state operation, I_{fw_avg} must be regulated to at least ($\Delta I_{ind}/2$). However, while this is enough for steady-state operation, in order to achieve a faster output dynamic response and better cross-regulation during light-to-heavy load steps, I_{fw_avg} may be regulated to higher levels based on the desired settling time for such

load steps. This comes at the expense of higher conduction losses, and thus there is a tradeoff between efficiency and the output dynamic performance. It is worth noting that the efficiency degradation due to higher I_{fw_avg} can be avoided in some cases without compromising the output dynamic performance if the change in the loads is known in advance. In such cases, I_{fw_avg} can be increased ahead of the anticipated load steps to achieve the best possible output dynamic response, and then later dropped in steady-state conditions to minimize losses.

3.2.3 Advantages of the DF-SIMO Topology

In addition to reducing the output capacitors (optionally to on-chip levels for output switching frequencies beyond 100 MHz), and improved dynamic response and cross-regulation compared to conventional single-frequency SIMO, the DF-SIMO topology offers the notable advantage of lending itself to a simplified implementation in nanometer CMOS. In fact, a key challenge in high switching frequency power converters in these technologies is the implementation of the power switches of the input stage. Since the input is typically a higher voltage (e.g. 1.8 V) than the voltage rating of the native transistors in these technologies (e.g. 1.2 V), alternative high-voltage transistors must be used for the power switches. These transistors have larger feature size and higher threshold voltage than the native transistors, and using them to realize the on-resistance required for a desired conduction loss results in larger transistor size and gate capacitance, which limits how fast they can be switched without causing excessively large switching losses and degraded efficiency. Although cascodes of the native transistors could be used to enable higher switching frequencies while also meeting the voltage rating of the transistors, the increased conduction losses that result from cascoding offsets the reduction in

switching losses. Moreover, driving cascodes of native transistors requires fairly complicated driver circuits, additional intermediate power supplies, and drain-, source-, and gate-to-bulk junction reliability continues to be a concern [26], [27]. The DF-SIMO topology eliminates these challenges since low switching frequency is retained at the input stage, and thus, single high-voltage transistors can be reliably used without negatively impacting efficiency and with fairly simple driver circuits.

CHAPTER 4

CONTROL LOOP AND SMALL-SIGNAL ANALYSIS

Although voltage-mode and current-mode schemes can be employed to regulate the average freewheeling current I_{fw_avg} through controlling the input stage, the design presented in chapter 5 is based on the current-mode PWM loop shown in Fig. 4.1. Thus, this chapter will focus on that particular scheme, where the single output case is considered first, and then the analysis is extended to multiple outputs. In this scheme, the average freewheeling current I_{fw_avg} is subtracted from the reference I_{fw_ref} to generate the error signal (I_p), which is then compensated and further subtracted an artificial ramp to eliminate sub-harmonic oscillations [28], [29]. The resulting signal is then compared to the inductor current to determine the input switching duty-cycle (dc_{in}) as illustrated in Fig. 4.2. To analyze the stability, the small-signal loop transfer function between I_{fw_avg} and the error signal (I_p) must be obtained. An approach for deriving the transfer function of similar loops used in boost converters with freewheeling current regulation was presented in [23]. However, it only considers conventional SIMO boost topologies (i.e. same input and output switching frequencies), and applying it directly to the DF-SIMO buck topology results in a very tedious and complicated analysis. In this thesis, I propose a modified approach that greatly simplifies obtaining the loop transfer function in the DF-SIMO buck case [25].

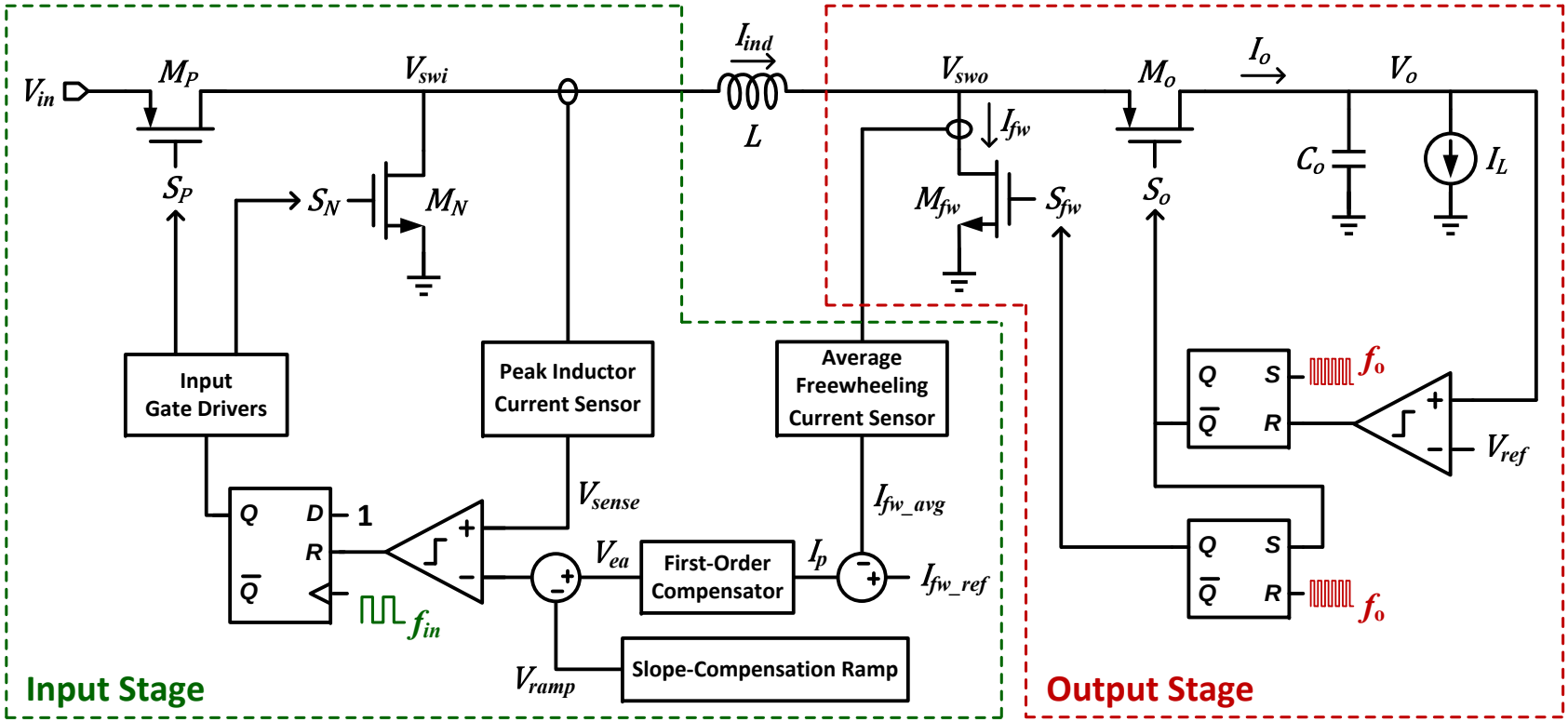


Figure 4.1. The DF topology with one output and a freewheeling switch, where the average freewheeling current is regulated by the input stage using a low-frequency current-mode PWM control loop.

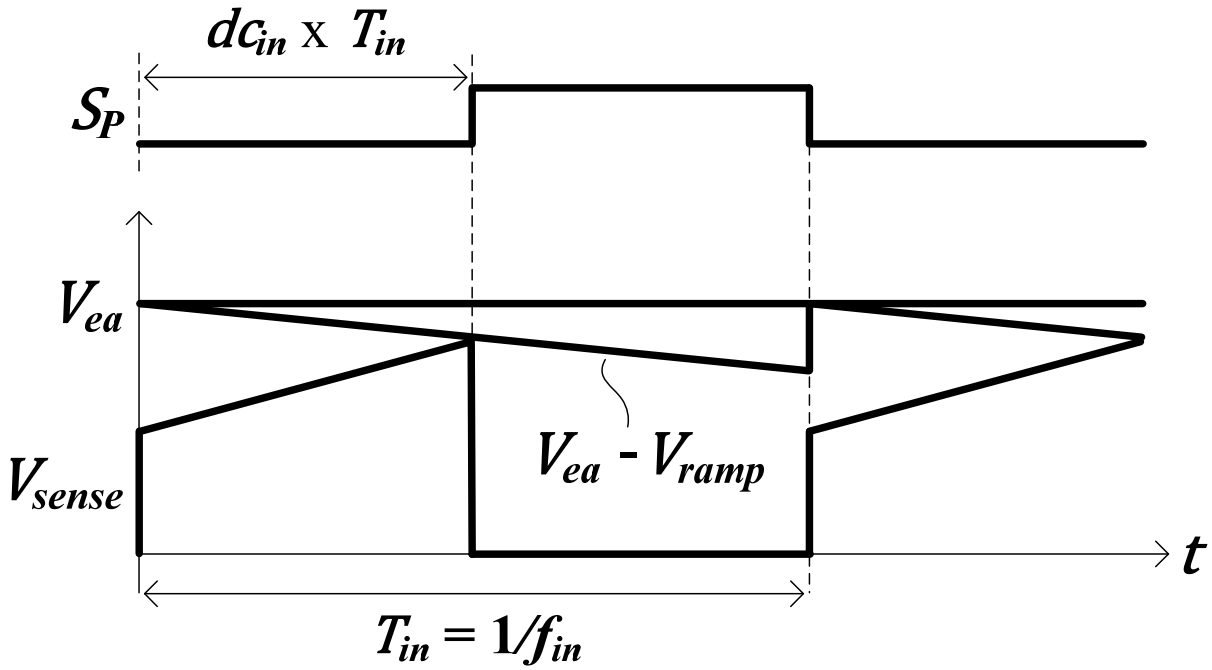


Figure 4.2. Current-mode PWM control loop to determine the input switching duty-cycle.

To aid with the derivation of the loop transfer function, the timing diagram of the single output case is shown in Fig. 4.3, where f_o is assumed to be synchronized to f_{in} and 4 times its frequency to simplify the drawing. The analysis is the same if the two frequencies are not synchronized or integer multiple of each other since a periodic steady-state will always be reached. Each output switching period (T_o) is divided among the output switch (M_o) and the freewheeling switch (M_{fw}), where (I_o) and (I_{fw}) are the instantaneous currents flowing in M_o and M_{fw} respectively. Since the total charge passed to the output every T_o is the same (due to comparator-based control), the area segments A_1 to A_4 in Fig. 4.3 are all equal to $(I_L \times T_o)$. Moreover, since the average freewheeling current I_{fw_avg} is regulated by the input control loop, the sum of the area segments B_1 to B_4 is equal to $\left(I_{fw\_ref} \times T_{in}\right)$, where T_{in} is the input

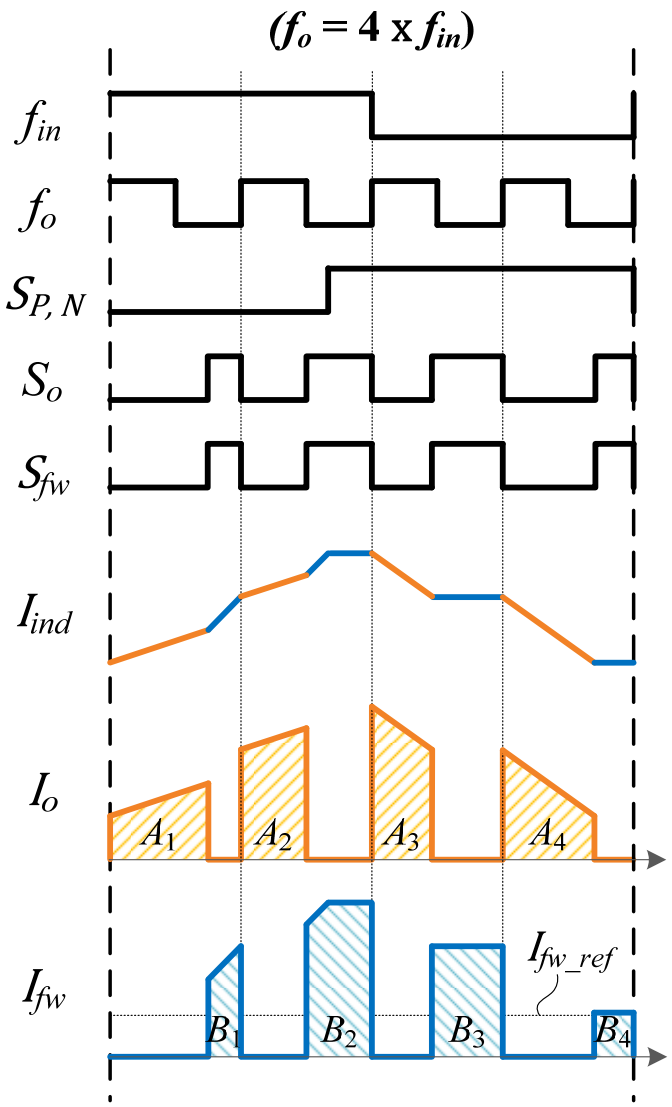


Figure 4.3. Timing diagram showing the various control signals, inductor current, freewheeling current, and output current for the circuit shown in Fig. 4.1.

switching period. The approach presented in [16] for conventional SIMO boost topologies relies on deriving a mathematical description for every segment of the inductor current during the input switching period. Applying this approach to the DF-SIMO topology produces a very large number of segments since the output switching frequency is much higher than the input, which significantly complicates the analysis. (e.g. 120 segments if input and output switching

frequencies are 2 MHz and 120 MHz respectively) However, at moderate to heavy loads, it can be assumed in the DF-SIMO case that the inductor's average current is significantly larger than its current ripple. Moreover, since the freewheeling current is always regulated to be higher than half the inductor current ripple, the assumption is further justified. In this case, the inductor current in Fig. 4.3 can be approximated as shown in Fig. 4.4, where all the similar segments (in terms of slope) are lumped together into a single composite segment. As a result, only 4

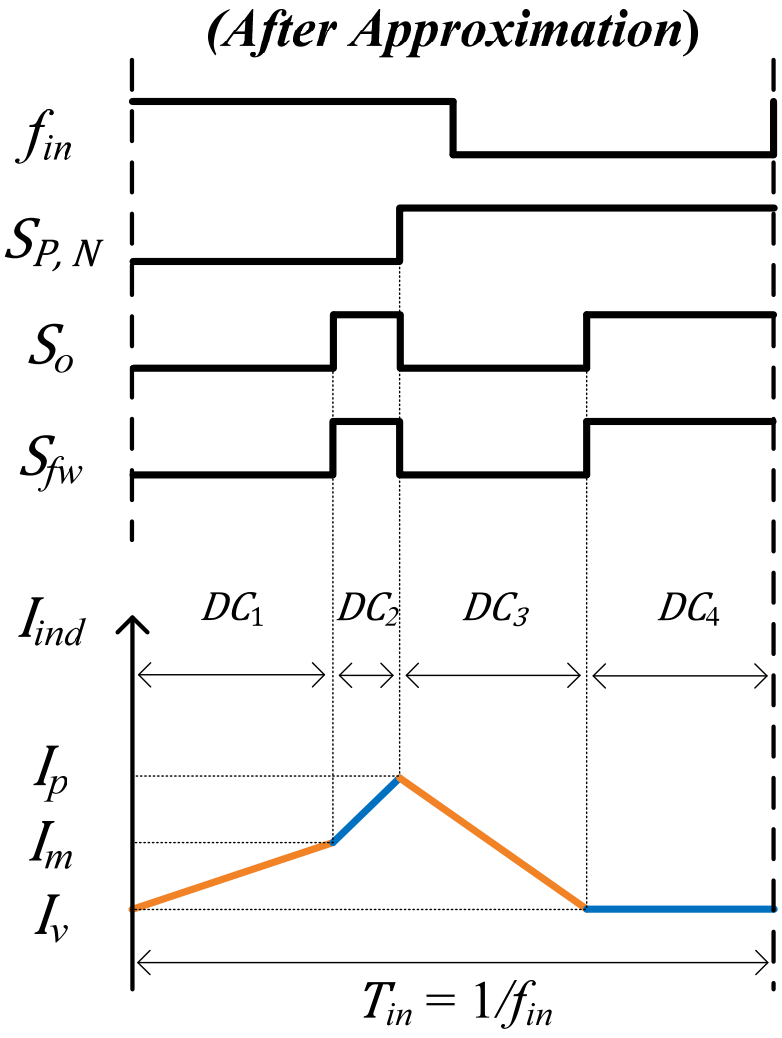


Figure 4.4. Timing diagram after lumping similar current segments together.

segments remain in the approximated inductor current profile, which can now be described in terms of only 3 current levels (i_v, i_m, and i_p) and 4 duty-cycles (dc_1, dc_2, dc_3, and dc_4) regardless of the actual ratio between the input and output switching frequencies. Therefore, the duty-cycles can be written as:

$$dc_1 = \frac{Lf_{in}}{(V_{in} - V_o)}(i_m - i_v) \tag{4.1}$$

$$dc_2 = \frac{Lf_{in}}{V_{in}}(i_p - i_m) \tag{4.2}$$

$$dc_3 = \frac{Lf_{in}}{V_o}(i_p - i_v) \tag{4.3}$$

$$dc_4 = 1 - dc_1 - dc_2 - dc_3 \tag{4.4}$$

where V_{in} and V_o are the input and output voltages, and L is the inductor value. Moreover, the freewheeling and output currents averaged over the input switching period can be written as:

$$i_{fw\_avg} = \frac{1}{2}(i_p + i_m)dc_2 + i_v dc_4 \tag{4.5}$$

$$i_{o\_avg} = \frac{1}{2}(i_v + i_m)dc_1 + \frac{1}{2}(i_p + i_v)dc_3 \tag{4.6}$$

Since the output charge is regulated every T_o, the following relationships are also true:

$$i_{o\_avg} = \frac{1}{2}(i_v + i_m)\frac{dc_1}{(dc_1 + dc_2)} \tag{4.7}$$

$$i_{o\_avg} = \frac{1}{2}(i_p + i_v)\frac{dc_3}{(dc_3 + dc_4)} \tag{4.8}$$

Small-signal perturbations can then be introduced to all the parameters in Eq. (4.1)–(4.8) as follows:

$$dc_1 = DC_1 + \widehat{dc}_1$$

$$dc_2 = DC_2 + \widehat{dc}_2$$

$$dc_3 = DC_3 + \widehat{dc}_3$$

$$dc_4 = DC_4 + \widehat{dc}_4$$

$$i_{o\_avg} = I_{o\_avg} + \hat{\imath}_{o\_avg}$$

$$i_{fw\_avg} = I_{fw\_avg} + \hat{\imath}_{fw\_avg}$$

$$i_v = I_v + \hat{\imath}_v$$

$$i_m = I_m + \hat{\imath}_m$$

$$i_p = I_p + \hat{\imath}_p \tag{4.9}$$

where the parameters in capital letters are the quiescent components, and the parameters with a hat are the small-signal components. As i_{o_avg} is regulated by the output stage (much faster than the input stage control loop bandwidth), its small-signal component $\hat{\imath}_{o\_avg}$ is always zero, while its quiescent component is equal to I_L. Moreover, since the input loop regulates i_{fw_avg}, its quiescent component is I_{fw_ref}. Combining Eq. (4.1) to (4.8), the following simultaneous equations for the quiescent components of i_v, i_m, and i_p can be derived for a given I_L and I_{fw_ref}:

$$\frac{1}{2} \times \left[\frac{(I_m^2 - I_v^2)}{(I_p - I_v) - \frac{V_o}{V_{in}}(I_p - I_m)} \right] = I_L \tag{4.10}$$

$$\frac{1}{2}\times\left[\frac{\frac{\left(I_p^2-I_v^2\right)}{V_o}}{\frac{1}{Lf_{in}}-\frac{(I_m-I_v)}{(V_{in}-V_o)}-\frac{\left(I_p-I_m\right)}{V_{in}}}\right]=I_L \tag{4.11}$$

$$Lf_{in}\times\left[\frac{\left(I_p^2-I_m^2\right)}{2V_{in}}+\frac{I_v}{Lf_{in}}-\frac{(I_m-I_v)I_v}{(V_{in}-V_o)}-\frac{\left(I_p-I_m\right)I_v}{V_{in}}-\frac{\left(I_p-I_v\right)I_v}{V_o}\right]=I_{fw\_ref} \tag{4.12}$$

These simultaneous equations can be solved numerically; and using linearization techniques on Eq. (4.1)–(4.9), the small-signal loop transfer function $G(s)$ can then be written as:

$$G(s)=\frac{\hat{\imath}_{fw\_avg}}{\hat{\imath}_p}=k_9+k_8\left[\frac{\frac{k_3}{k_2}-\frac{k_6}{k_5}}{\frac{k_1}{k_2}-\frac{k_4}{k_5}}\right]+k_7\left[\frac{\frac{k_3}{k_1}-\frac{k_6}{k_4}}{\frac{k_2}{k_1}-\frac{k_5}{k_4}}\right] \tag{4.13}$$

where

$$k_1=\frac{-V_{in}I_v}{(V_{in}-V_o)V_o}$$

$$k_2=\frac{I_m}{(V_{in}-V_o)}$$

$$k_3=\frac{-I_p}{V_o}$$

$$k_4=\frac{(I_L-I_m)}{(V_{in}-V_o)}$$

$$k_5=\frac{(I_m-I_L)}{(V_{in}-V_o)}+\frac{I_L}{V_{in}}$$

$$k_6=\frac{-I_L}{V_{in}}$$

$$k_7 = Lf_{in} \times \left[\frac{(I_v - I_m)}{V_{in}} - \frac{I_v}{(V_{in} - V_o)}\right]$$

$$k_8 = 1 - Lf_{in} \times \left[\frac{(I_m - 2I_v)}{(V_{in} - V_o)} - \frac{(I_p - I_m)}{V_{in}} - \frac{(I_p - 2I_v)}{V_o}\right]$$

$$k_9 = Lf_{in} \times \left[\frac{(I_p - I_v)}{V_{in}} - \frac{I_v}{V_o}\right] \quad (4.14)$$

Eq. (4.13) and (4.14) show that the loop transfer function does not contain any poles or zeros (just a DC gain) despite the fact that the inductor is operating in CCM. This result can be intuitively understood by taking into consideration two factors. First, since the input stage uses current-mode control, the inductor current is being regulated every cycle of the input switching frequency, which is normally 5 to 10 times larger than the bandwidth of the input control loop. Therefore, the inductor appears to the input control loop as a DC current source, which reduces the order of the system to first order rather than second order. This is generally true for current-mode controllers [28], [29]. Second, since the output is regulated using comparator-based control (rather than PWM or PFM control), the output current is also regulated every cycle of the output switching frequency, and thus appears to the much slower input control loop as if it is a constant DC current that is equal to the load current. This eliminates the effect of the output capacitor, and further reduces the order of the input control loop to zero. This is true for conventional SIMO converters (same input and output switching frequencies) with comparator-based control as demonstrated in the SIMO boost converter case in [16], but even more justified in the proposed DF-SIMO since the output switching frequency is much higher than the input switching frequency. However, the first-order low-pass compensator in Fig. 4.1 must still be used to

introduce a dominant load-independent pole to ensure stability and limit the unity gain frequency of the loop to about $(1/10)$ to $(1/5)$ the input switching frequency.

To extend the analysis to multiple outputs, the weighted average voltage of all the outputs, which is presented in [16] for conventional SIMO boost topologies, can be also employed in the DF-SIMO to yield the same transfer function form as the single output case. The weighted average output voltages can be based on either the output duty-cycles, or the output loads as follows:

$$\langle V_o \rangle_{dc} = \sum_{i=1}^{n} V_{o(i)} dc_{o(i)} \Big/ \sum_{i=1}^{n} dc_{o(i)}$$

$$\langle V_o \rangle_{I_L} = \sum_{i=1}^{n} V_{o(i)} I_{L(i)} \Big/ \sum_{i=1}^{n} I_{L(i)} \qquad (4.15)$$

where $V_{o(i)}$, $dc_{o(i)}$, and $I_{L(i)}$ are the steady-state output voltage, duty-cycle, and load current of the i^{th} output respectively, and n is the number of outputs.

CHAPTER 5

A LOW-POWER DF-SIMO IMPLEMENTATION

In this chapter, a dual-frequency single-inductor 5-output buck converter is designed and implemented in 45-nm digital CMOS process targeting low-power microcontroller SoCs as shown in Fig. 5.1 [25]. The converter operates from 1.8-V input and produces 5 outputs with the voltage range, maximum load, and on-chip output capacitance noted in Fig. 5.1 for each output. The 5th output is dedicated for the digital core of the microcontroller, while the 4th, 3rd, and 2nd outputs are dedicated for various other digital loads in the system. The 1st output is dedicated for various analog modules within the system that require a power supply higher than 1.2 V. The converter uses 2 MHz and 120 MHz for the input and output switching frequencies respectively. The input stage controller regulates the freewheeling current between 15 mA to 45 mA in order to enable fast output dynamic response as explained in section 3.2.2. Some design details are discussed in the following subsections.

5.1 Power Switches and Output Gate Drivers

Since the input is 1.8 V, the power switches M_P and M_N are implemented using a single 1.8-V rated transistor for each switch as shown in Fig. 5.1, which is possible with acceptable switching losses due to the low input switching frequency. For the output stage, the voltage profile of V_{swo}, which follows the output levels as shown in Fig. 5.2, is critical for determining the type of devices that can be used as output and freewheeling power switches. Since $V_{o(1)}$ is

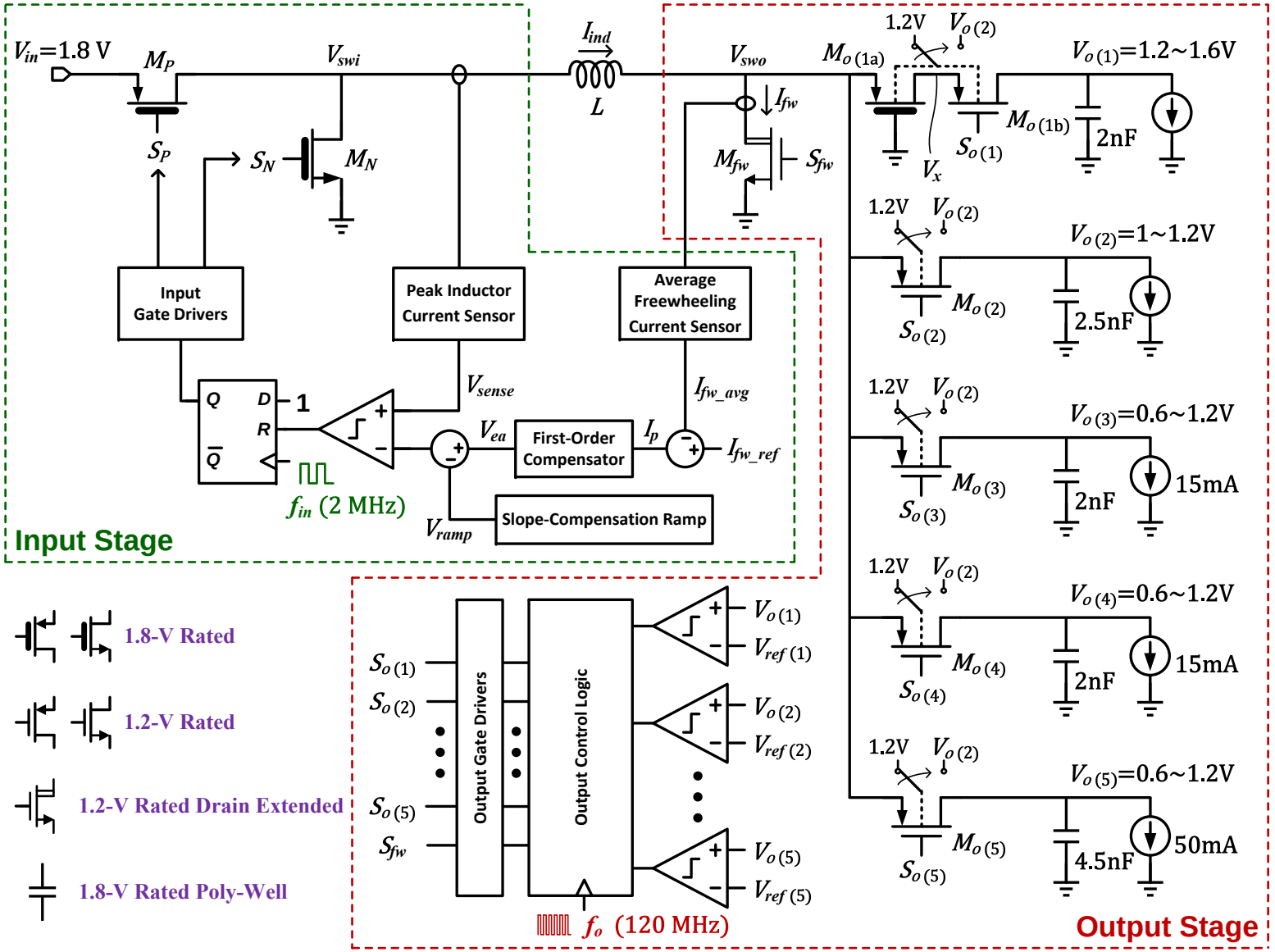


Figure 5.1. Block diagram of a dual-frequency single-inductor 5-output buck converter implemented in 45-nm digital CMOS.

higher than 1.2 V, the freewheeling switch (M_{fw}) is implemented using a 1.2-V rated drain-extended NMOS that is rated for up to 1.8 V at its drain-to-source junction. For the last 4 outputs (less than 1.2 V), the switches $M_{o(2)}$ to $M_{o(5)}$ are implemented using 1.2-V rated PMOS devices as they offer the smallest switching losses. However, their gate driver signals $S_{o(2)}$ to $S_{o(5)}$ must be designed to ensure proper on/off operation while preserving the 1.2-V rating. For that reason, the voltage levels of the signal $S_{o(2)}$ is designed as shown in Fig. 5.2 (similar levels are used for $S_{o(3)}$ to $S_{o(5)}$). If the 1st output is connected ($V_{swo} > 1.2$ V), the signals $S_{o(2)}$ to $S_{o(5)}$ are set to $V_{o(1)}$ to completely turn off $M_{o(2)}$ to $M_{o(5)}$. If one of the last 4 outputs is connected ($V_{swo} \leq 1.2$ V), $S_{o(2)}$ to $S_{o(5)}$ are set to either 1.2 V or zero depending on which of the last 4 outputs is connected. If the freewheeling switch is active ($V_{swo} \approx 0$ V), $S_{o(2)}$ to $S_{o(5)}$ are set to 1.2 V. With this strategy, the differential voltage between any of the terminals of $M_{o(2)}$ to $M_{o(5)}$ is 1.2 V or less at any time. For the 1st output (higher than 1.2 V), the switch is implemented using a cascode of a 1.8-V rated and a 1.2-V rated PMOS devices ($M_{o(1a)}$ and $M_{o(1b)}$ respectively). The gate of $M_{o(1a)}$ is always connected to zero, while the gate driver signal $S_{o(1)}$ of $M_{o(1b)}$ toggles between $V_{o(1)}$ and $(V_{o(1)} - 1.2\text{ V})$, which produces the voltage profile at the node V_x shown in Fig. 5.2. Since node V_x is clamped to the threshold voltage of $M_{o(1a)}$ (~0.5 V) during the freewheeling period, this configuration ensures the voltage rating of $M_{o(1b)}$ is not violated at any time.

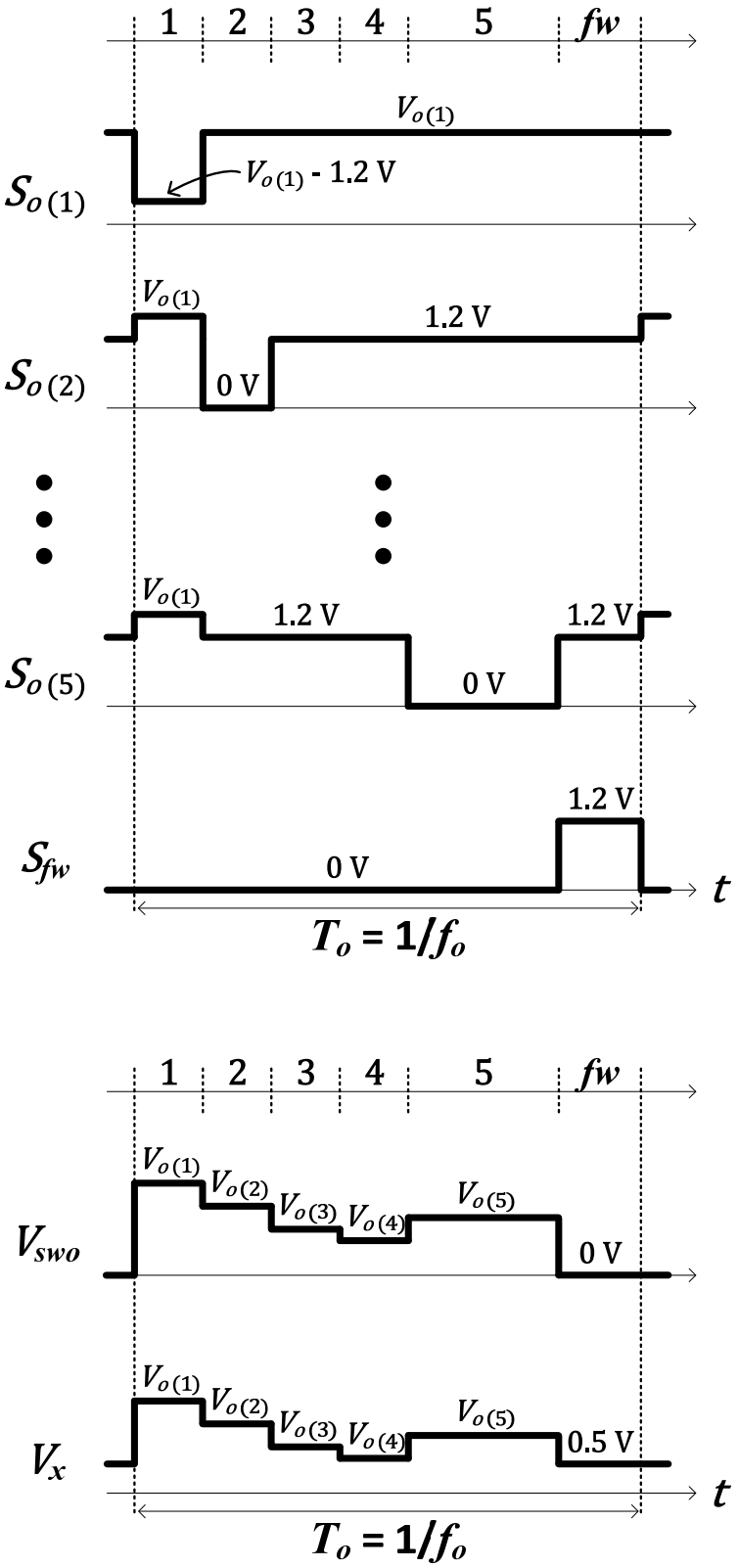


Figure 5.2. Timing diagram and voltage levels of critical nodes in the output stage.

To ensure that the body-diodes of all the output transistors never turn on, their bulks are connected to a temporary 1.2-V supply during startup, and then switched to $V_{o(2)}$ during normal operation. Although the body-diodes of the output transistors will be slightly forward-biased because V_{swo} can be as high as 1.6 V, no significant leakage is observed since the forward voltage of the body-diodes is over 0.7 V. In fact, this slight forward-biasing of the body-diodes of the output transistors reduces their on resistance, which helps improving efficiency. Moreover, $V_{o(1)}$ is first set to 1.2 V during startup until all the other outputs have reached their final levels (0.6–1.2 V), then it is regulated to its desired 1.2–1.6 V range. This ensures the drain-to-source voltages of all the output transistors never exceed their rated 1.2-V level. In order to generate the gate driver signals, $S_{o(1)}$ is first generated using the capacitively-coupled level shifter in [30] but with an additional stage to generate the complementary signal $\overline{S_{o(1)}}$ swinging between $V_{o(1)}$ and 0 V as shown in Fig. 5.3. Ideally, $S_{o(1)}$ swings between $V_{o(1)}$ and $\left(V_{o(1)} - 1.2\ \mathrm{V}\right)$, but due to the output load capacitor, the actual output swing is smaller depending on the ratio of the coupling capacitor (C_1) and the load capacitor. $S_{o(1)}$ and $\overline{S_{o(1)}}$ are then used by four identical copies of the circuit in Fig. 5.4 to generate the signals $S_{o(2)}$ to $S_{o(5)}$. 1.8-V rated devices are stacked in both drivers to support more than 1.2-V signaling. A single switching 1.8-V rated device could replace the cascoded configuration, but it results in higher switching and conduction losses based on the simulation in this process.

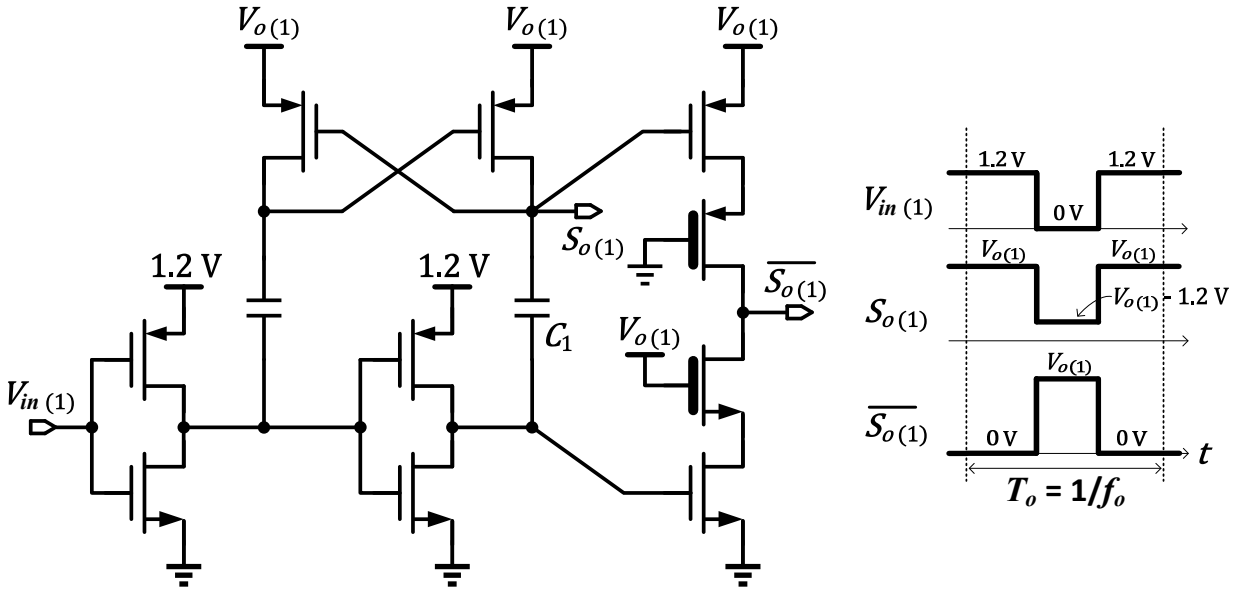


Figure 5.3. The gate driver circuit design and its timing diagrams for the 1st output (higher than 1.2 V).

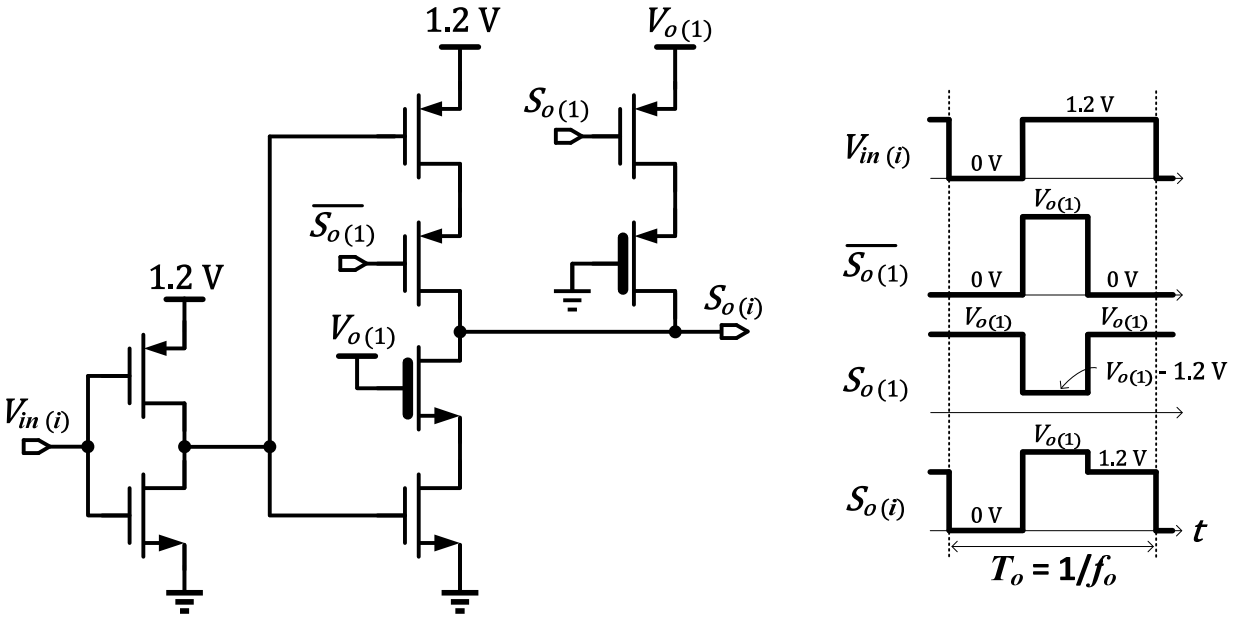


Figure 5.4. The gate driver circuit design and its timing diagrams for the 2nd, 3rd, 4th, and 5th outputs (1.2 V or less).

5.2 Inductor Current Sensing and Ramp Generation

As the input stage switches at low frequency, the standard high-side and low-side current sensors in Fig. 5.5 [31]–[37] are used to sense the inductor current. The error amplifiers force V_1 to track V_2, and V_3 to track V_4. Thus, the high-side current flowing through M_P is mirrored to M_{Ps} with the ratio set by the size between them (2000:1) when the high-side gate driver signal (S_P) is set to zero; similarly the low-side current flowing through M_N is mirrored to M_{Ns} with the same ratio when the low-side gate driver signal (S_N) is set to the input voltage. The sensed high-side current (I_{HS}) is then passing through the resistor (R_{sense}) to generate the corresponding voltage signal (V_{sense}) shown in Fig. 5.1. I_{HS} can also be easily combined with the sensed low-side current (I_{LS}) in the form of current to generate the full sensed inductor current.

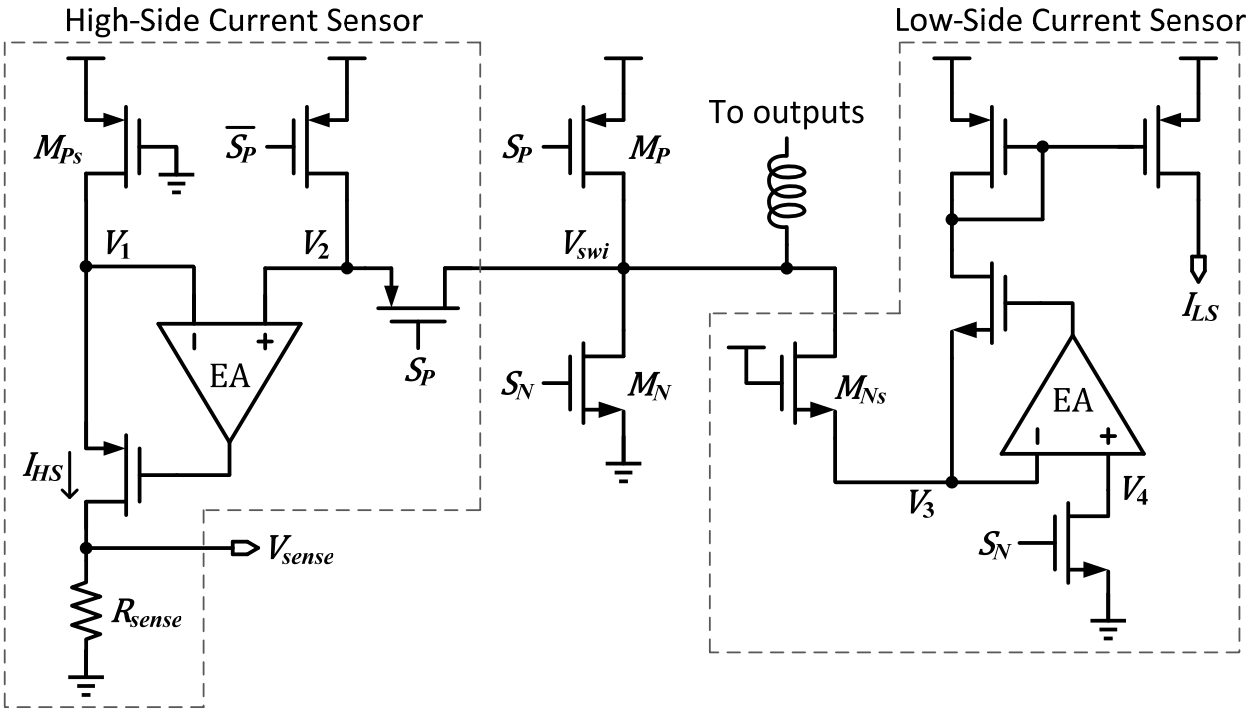


Figure 5.5. The high-side and low-side inductor current sensors.

Fig. 5.6 shows the schematic of the ramp signal generator. The frequency and magnitude of the ramp signal (V_{ramp}) is controlled by charging the capacitor (C_1) with a constant current source (I_1) and discharging it every input switching period. Although V_{ramp} is subtracted from the error signal (V_{ea}) generated by the first-order compensator in the form of voltage as shown in Fig. 5.1, it is easier to build a current adder in the real implementation. Therefore, a simple voltage-to-current converter (M_1, M_2 and R_1) is used [32] to generate the corresponding current signal (I_{ramp}), and then passing it through R_{sense} together with I_{HS} to form the combined voltage signal ($V_{sense} + V_{ramp}$) instead. The source follower M_1 acts as a dc level shifter in order to turn on the NMOS transistor M_2. A bias current (I_2) is added to remove the offset current caused by the level shifter.

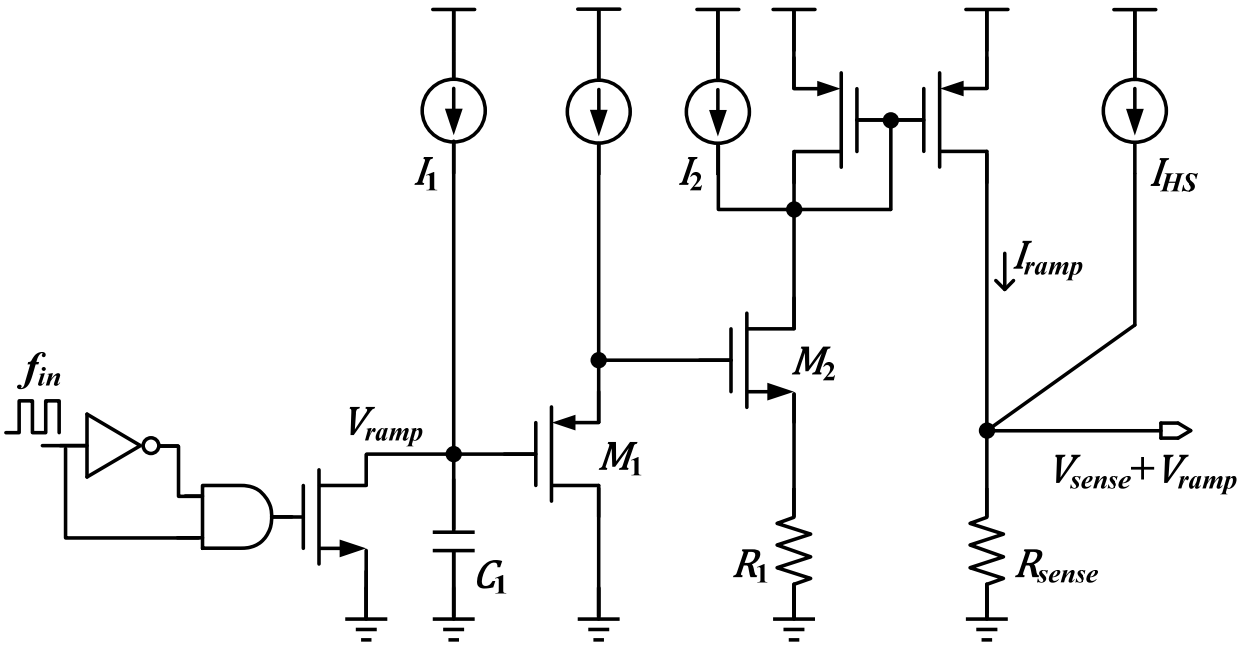


Figure 5.6. The artificial ramp generator used to eliminate sub-harmonic oscillations.

5.3 Freewheeling Current Sensing, Error Signal Generation, and Loop Compensation

As for the average freewheeling current sensing, please note that Fig. 4.1 and Fig. 5.1 are essentially conceptual. In the actual circuit implementation, the average freewheeling current is not directly sensed or explicitly represented as a physical signal. The average freewheeling current I_{fw_avg} and the first order loop compensation filter are both inherently realized by the charge pump circuit shown in Fig. 5.7 [25]. In this circuit, the sensed inductor current (I_{ind_sense}) is gated by the freewheeling switch driver signal S_{fw} to generate the switching current (I_{fw_sw}). The DC component of the difference between I_{fw_ref} and I_{fw_sw} (i.e. $I_{fw\_ref} - I_{fw\_avg}$) is extracted by the integrating capacitor (C_{ea}), which generates the error signal V_{ea} and introduces the first-order low-pass compensation function needed to limit the bandwidth of the input control loop. The size of the capacitor is chosen such that the GBW product of the loop is about $(1/10)$ the input switching frequency.

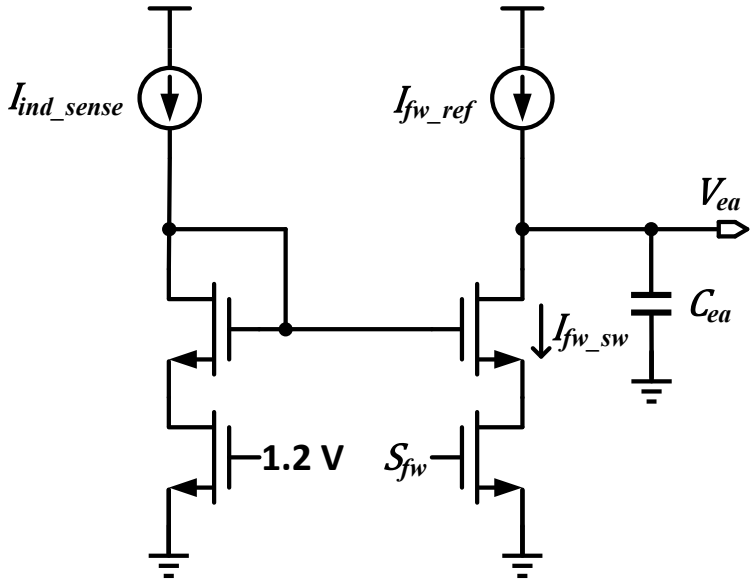


Figure 5.7. The charge pump used to realize the average freewheeling current sensor and the first-order loop compensator.

5.4 Comparators and D Flip-Flops

Comparators are needed in both the input and output stages. Since they operate at two different switching frequencies, two structures are designed to meet their requirements for different purposes. In the input stage which runs at 2 MHz, the comparator is used to determine the duty-cycle of the PWM control signal for the power generation switches, and thus a low-speed high-gain comparator with positive feedback [32], [38] is implemented as shown in Fig. 5.8. The gain of the positive feedback stage (M_1–M_6) can be expressed as:

$$A_d = \sqrt{\frac{\mu_p (W/L)_1}{\mu_n (W/L)_3}} \frac{1}{1-\alpha} \tag{5.1}$$

where $\alpha = (W/L)_5/(W/L)_3$ is the positive feedback factor which is usually chosen between

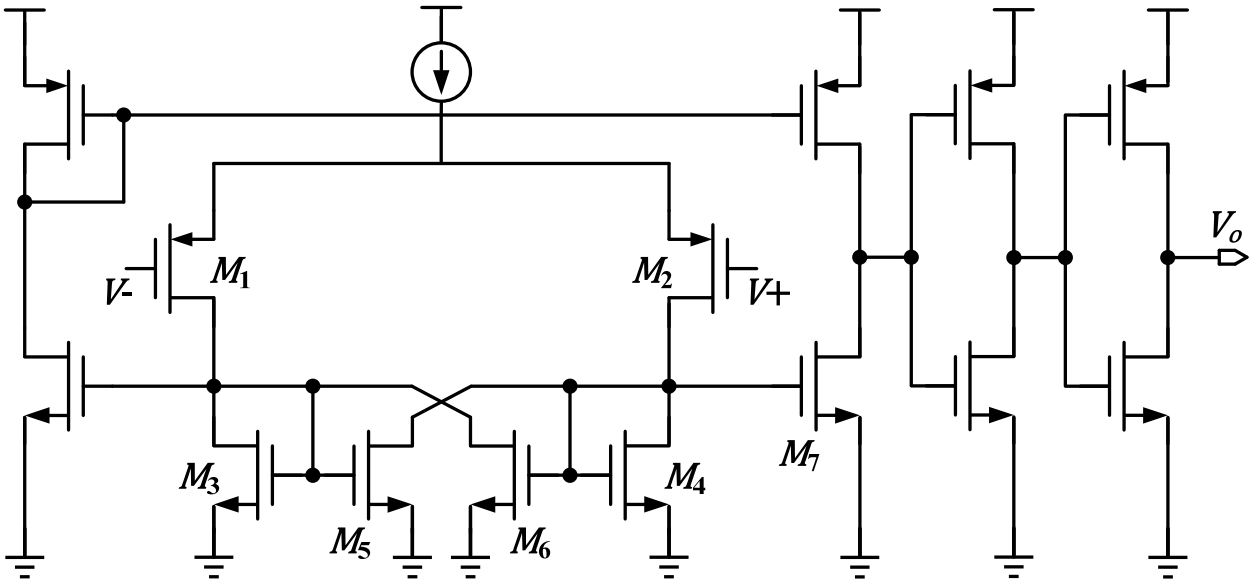


Figure 5.8. The comparator with positive feedback used for the input stage.

0.75 to 0.9. The response time is limited by the parasitic capacitance of the load so two inverters are added to serve as the post driver stage to separate M_7 and the load for a faster response.

Since the output stage operates at a much higher switching frequency, high-speed comparators are needed to minimize the delay. This is more critical for multiple-output topologies, because each output is allocated an even smaller amount of the output switching period. For example, if the output switching frequency is 100 MHz and there are five outputs with the same load current, each output occupies less than 2 ns due to some period has to be assigned to the freewheeling switch. The comparators and digital logics have to determine which output or freewheeling switches to turn on and off promptly within 2 ns. Thus, the overall delay from the comparators, control logics and drivers will limit the maximum switching frequency for the output stage. This phenomenon will be further discussed in section 5.5. The schematic of the high-speed comparators implemented for this work is shown in Fig. 5.9. This comparator is designed with two low-gain high-bandwidth preamplifiers that drive the latch stage, followed by the post-amplifier. The gain for each preamplifier is about 2 to 3 times. The simulated delay for a 50-mV_{PP}, 125-MHz sawtooth input signal is around 200 ps.

As for the D flip-flops in the control logics of the output stage, customized design is used in order to minimize the propagation delay when clock, set or reset signal is triggered for the same reason explained above. The schematic is shown in Fig. 5.10 and the simulated delay is between 20 to 40 ps for different conditions.

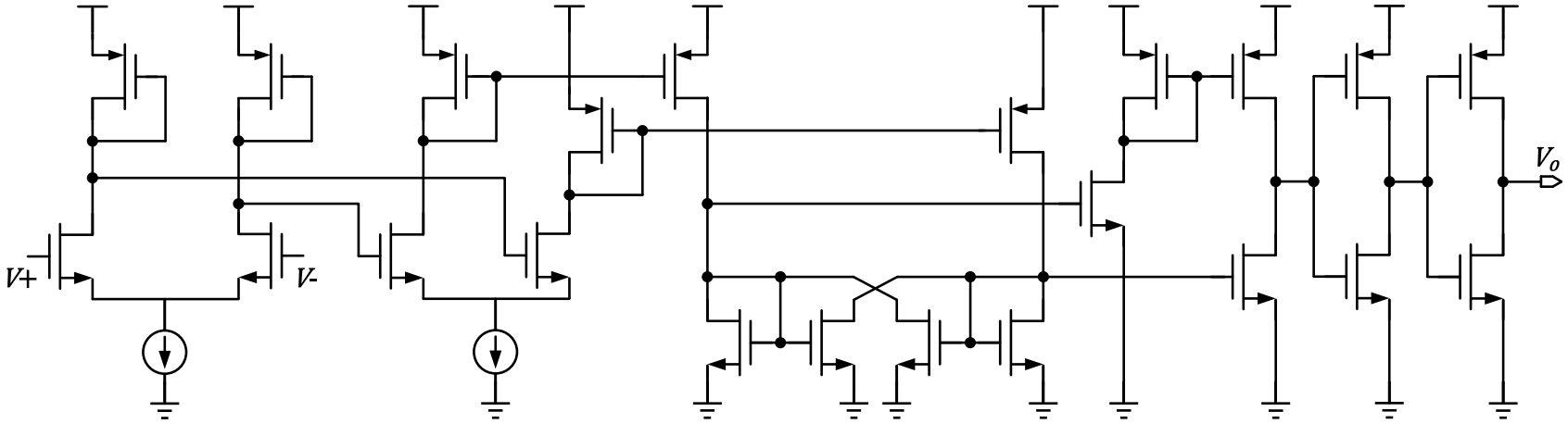


Figure 5.9. The high-speed comparator used for the output stage.

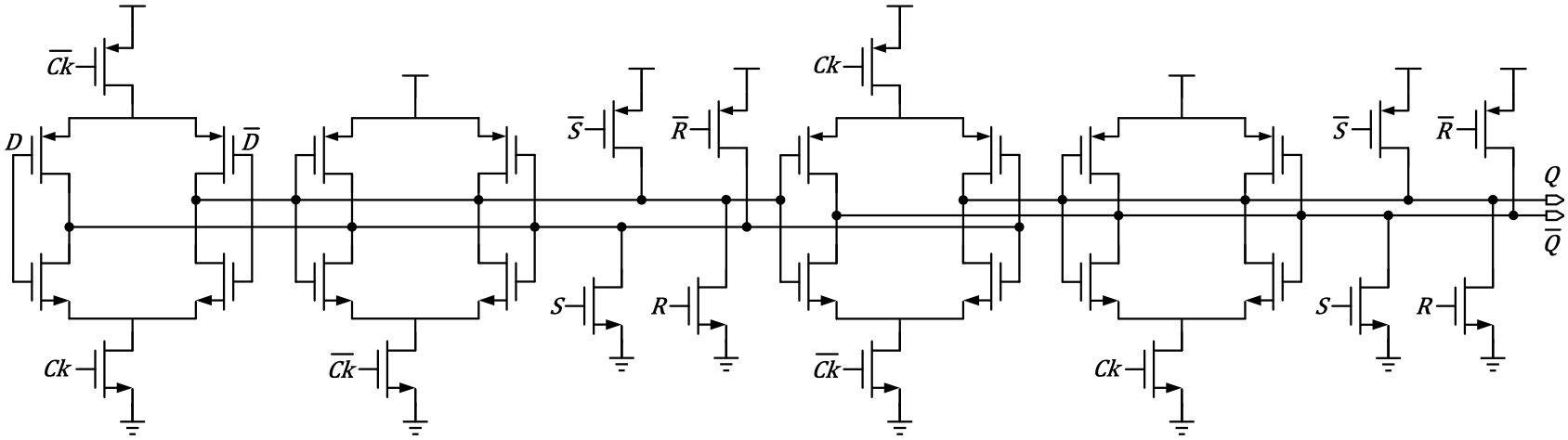


Figure 5.10. The D flip-flop used in the control logics for the output stage.

5.5 Output-Skipping and Output-Reordering Logics

Since all the outputs are served sequentially within each output switching period, the i^{th} output voltage ($V_{o(i)}$) must cross its reference level ($V_{ref(i)}$) before it is disconnected and the inductor current is allowed to be routed to the $(i+1)^{th}$ output. However, due to comparator, control logics and driver delay (T_d), the i^{th} output will not be immediately disconnected and will continue to charge beyond its reference level for a brief period of time as shown in Fig. 5.11(a). If the load current at this particular output is relatively small, there is a potential that by the new switching cycle its voltage will not have yet dropped below $V_{ref(i)}$ as shown in Fig. 5.11(b). In this scenario, this output will continue to be disconnected until it drops below $V_{ref(i)}$, which will prevent the subsequent outputs (including the freewheeling switch) from being served, and the inductor will have to turn on the body diodes of the output power switches to dissipate its energy. Although such scenario is possible in any conventional comparator-based SIMO topology (at very light loads), it happens in the DF-SIMO topology at moderate load levels due to the fast output switching frequency. This can be somewhat mitigated by minimizing the comparator and driver delay at the expense of higher power consumption. However, the DF-SIMO topology adopts an alternative output-skipping approach to this problem as shown in Fig. 5.11(b). In this scheme, if the i^{th} output turn comes within any switching period while its comparator is still indicating that its level is higher than its reference, then the comparator associated with the $(i-1)^{th}$ output is used to initiate routing the inductor current to the $(i+1)^{th}$ output, and the i^{th} output is completely skipped. This skipping continues for as many output switching cycles as needed until the i^{th} output drops below its reference (which is a function of the load current and the holding capacitor of this particular output). As a result, the effective switching frequency of

the i^{th} output is reduced based on its load current, i.e. PFM control. This output-skipping approach avoids having to design excessively fast and power-hungry comparator and gate driver circuits, and scales down the switching losses at any output with the load current, which helps improving efficiency.

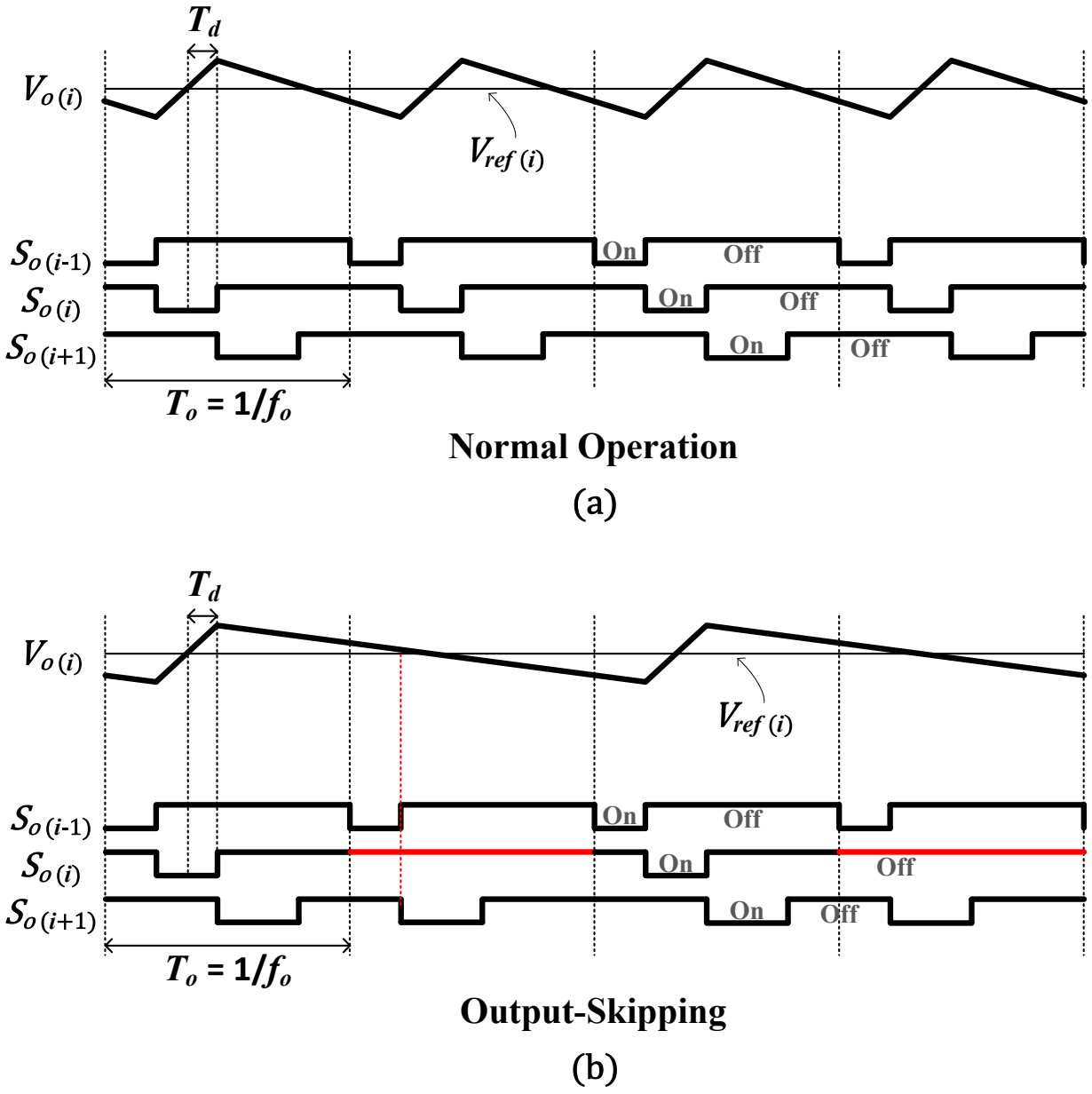


Figure 5.11. Output-skipping logic is enabled during lighter loads.

Moreover, if the load at one of the outputs suddenly rises, its local duty-cycle must increase to accommodate the additional load, and if the load step is very large, its duty-cycle may extend to the entire output switching period. This deprives the outputs that come later in the sequence from the inductor charge, which leads to poor cross regulation. To mitigate that, an additional output-reordering function is implemented to modify the output sequence such that the output with a positive load step is always moved to the end of the sequence. As a result, the duty-cycle of this particular output can only intrude into the duty-cycle of the freewheeling switch without affecting any of the other outputs as shown in Fig. 5.12, where only 3 outputs are used for simplicity.

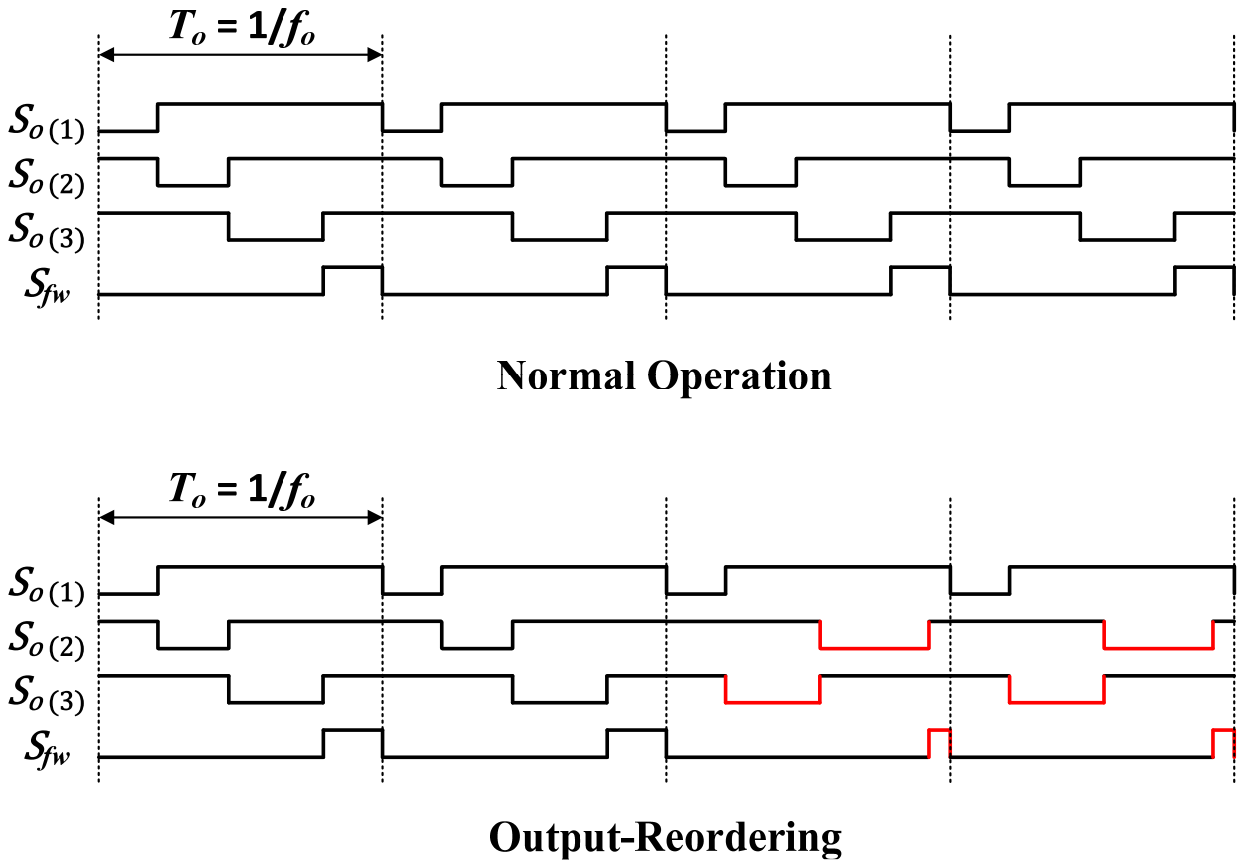


Figure 5.12. Output-reordering logic is enabled for light-to-heavy load steps on the 2nd output.

5.6 Simulation Results

5.6.1 Transient Response during Startup

(f_{in}: 2 MHz; f_o: 120 MHz; I_{fw_ref}: 15 mA; $V_{o(1)}$: 1.6 V, 15 mA; $V_{o(2)}$: 1.2 V, 15 mA; $V_{o(3)}$: 1.2 V, 15 mA; $V_{o(4)}$: 0.6 V, 15 mA; $V_{o(5)}$: 0.9 V, 50 mA)

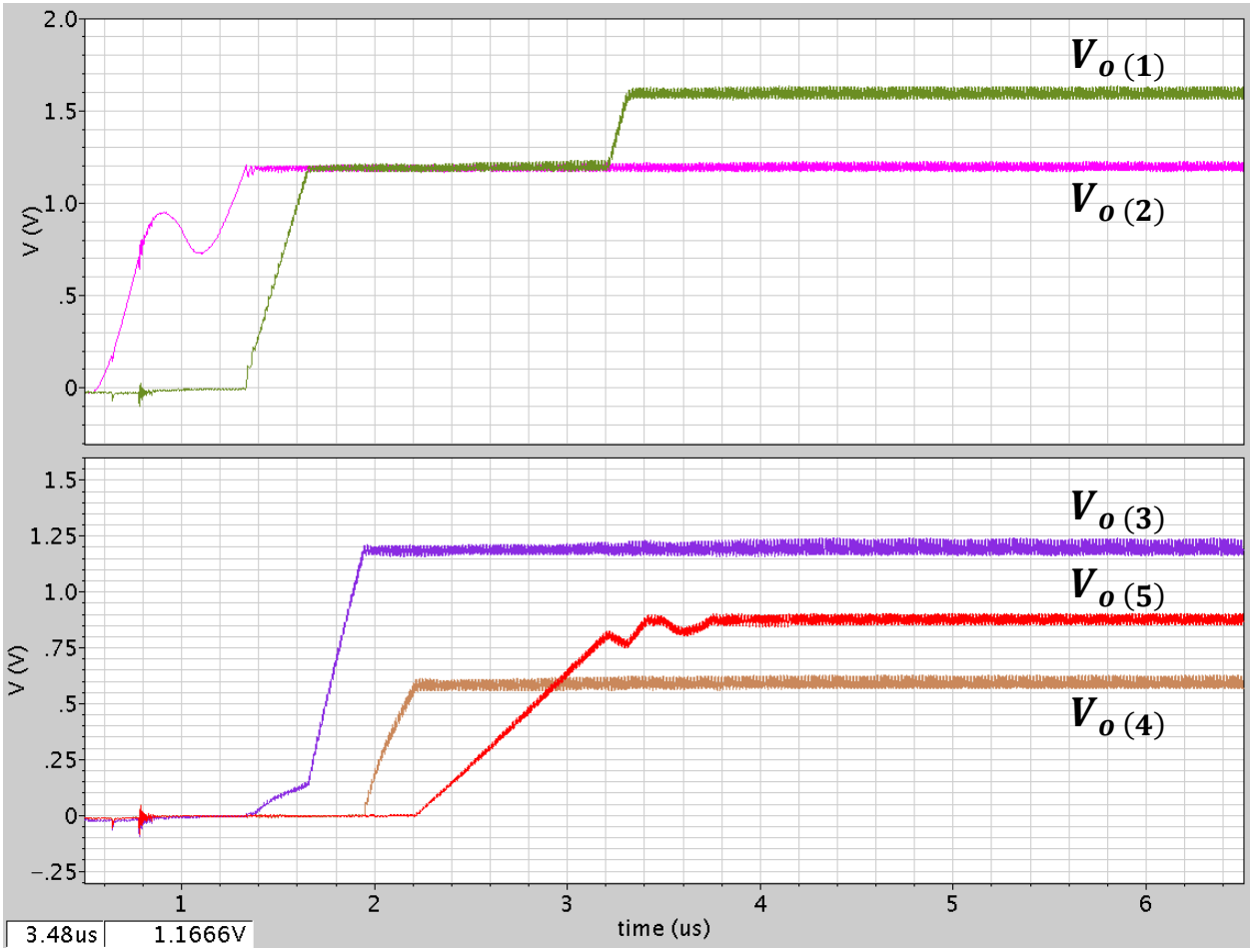


Figure 5.13. The simulated output waveforms during startup.

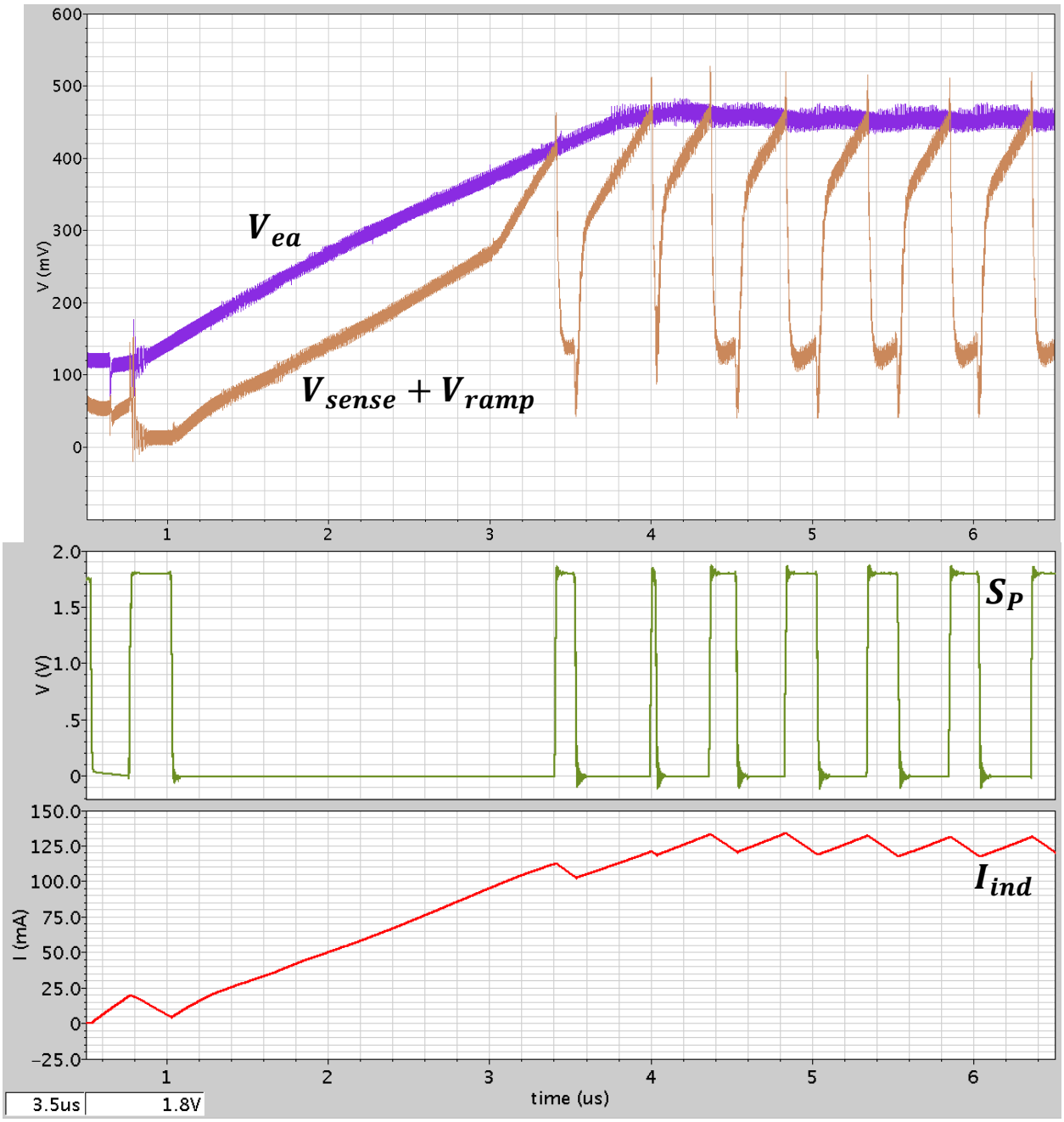


Figure 5.14. The simulated error and sensed signals which determine the input duty-cycle.

5.6.2 Switching Nodes in Steady-State

(f_{in}: 2 MHz; f_o: 120 MHz; I_{fw_ref}: 15 mA; $V_{o(1)}$: 1.6 V, 15 mA; $V_{o(2)}$: 1.2 V, 15 mA; $V_{o(3)}$: 1.2 V, 15 mA; $V_{o(4)}$: 0.6 V, 15 mA; $V_{o(5)}$: 0.9 V, 50 mA)

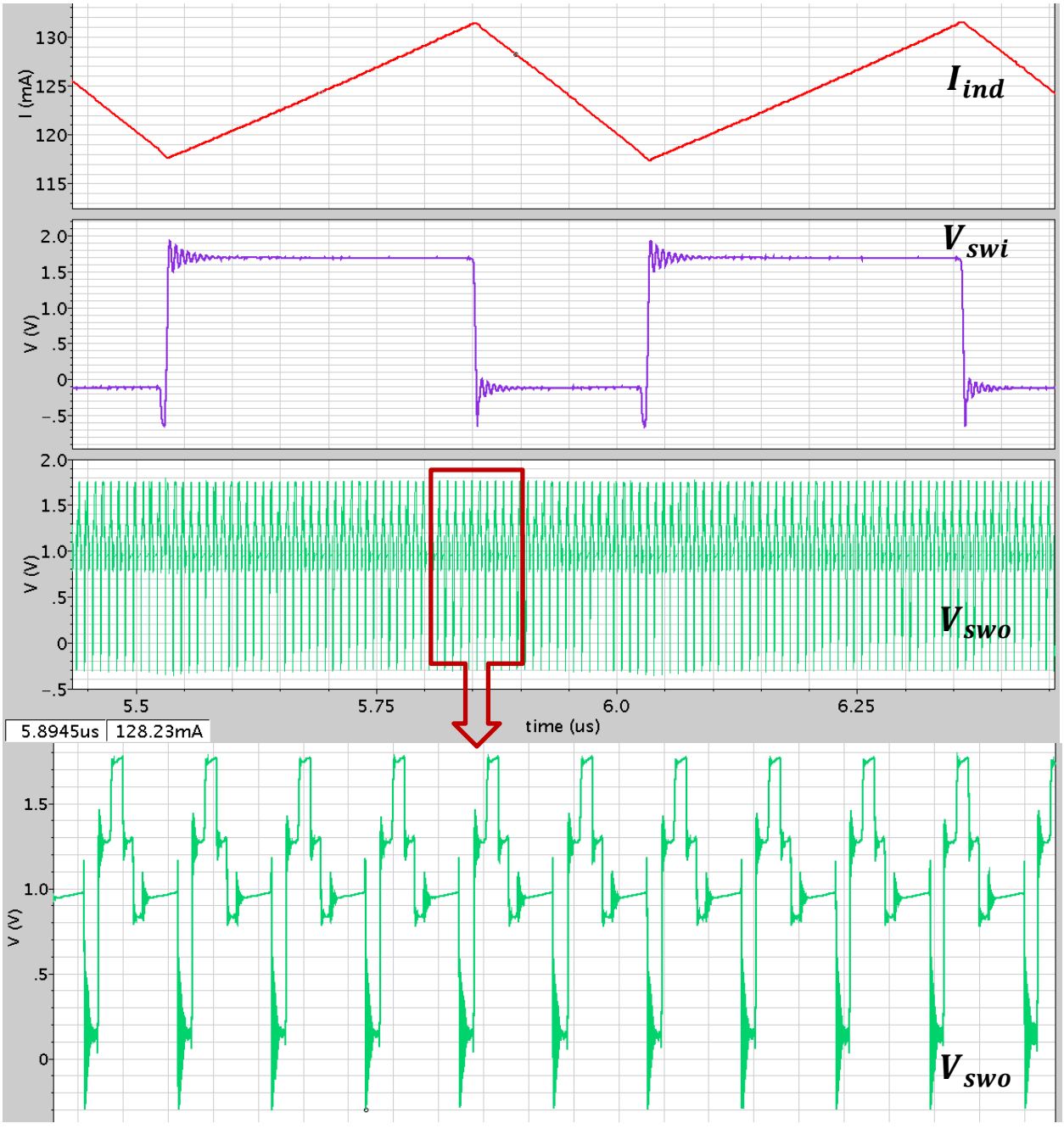


Figure 5.15. The simulated input switching node, inductor current, and output switching node.

5.6.3 Load Regulation

(f_{in}: 2 MHz; f_o: 120 MHz; I_{fw_ref}: 35 mA; $V_{o(1)}$: 1.6 V, 15 mA; $V_{o(2)}$: 1.1 V, 15 mA; $V_{o(3)}$: 1 V, 15 mA; $V_{o(4)}$: 0.8 V, 15 mA; $V_{o(5)}$: 1.2 V, 50 → 35 → 50 mA)

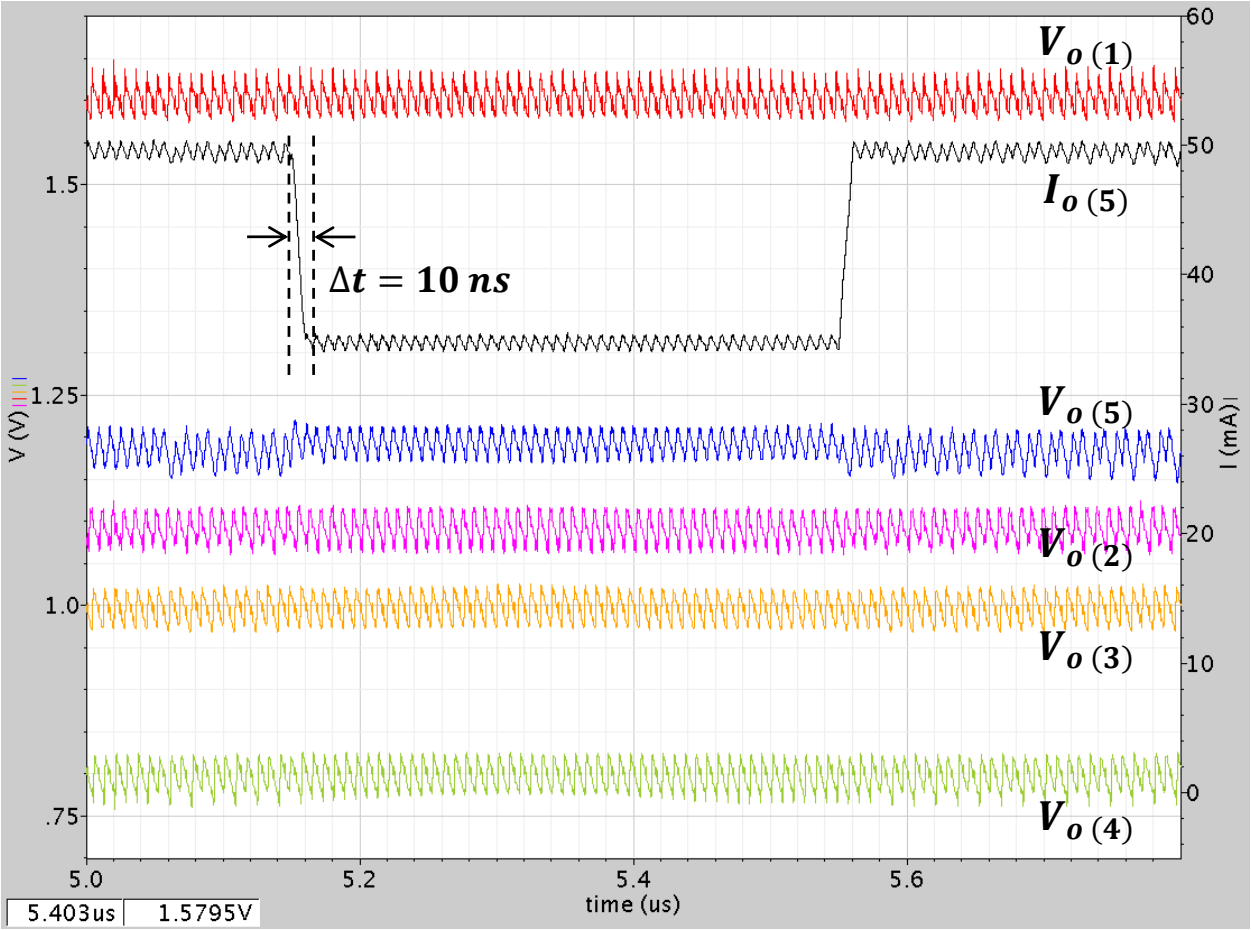


Figure 5.16. Transient response of the 5th output with a ±15-mA load step showing fast dynamic performance and excellent cross regulation between all the outputs.

5.6.4 Dynamic Voltage Scaling

(f_{in}: 2 MHz; f_o: 120 MHz; I_{fw_ref}: 45 mA; $V_{o(1)}$: 1.6 V, 15 mA; $V_{o(2)}$: 1.1 V, 15 mA; $V_{o(3)}$: 1 V, 15 mA; $V_{o(4)}$: 0.8 V, 15 mA; $V_{o(5)}$: 1.2 V, 50 mA → 0.6 V, 25 mA → 1.2 V, 50 mA)

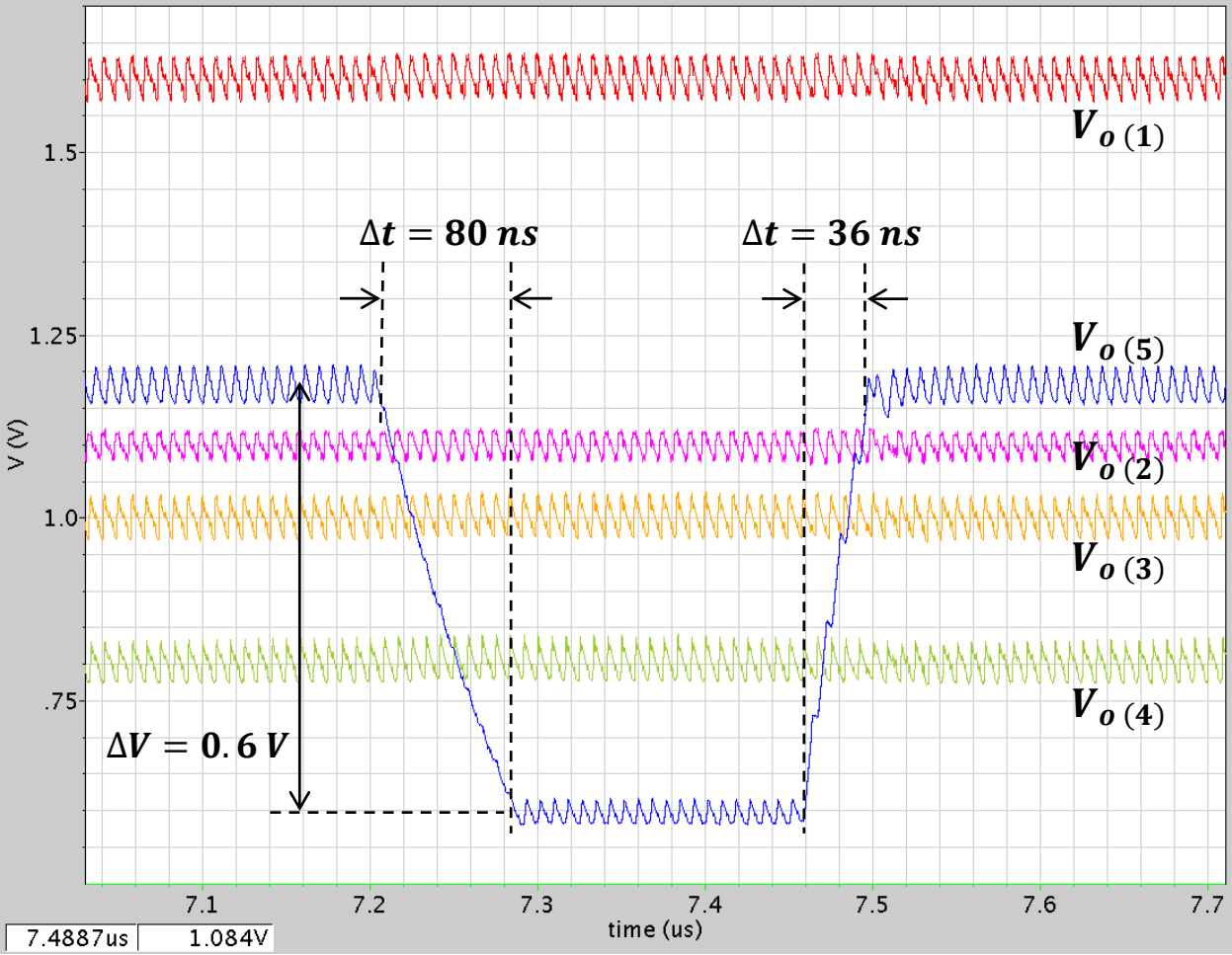


Figure 5.17. Transient response of the 5th output with a ±600-mV voltage change request showing fast dynamic performance and excellent cross regulation between all the outputs.

CHAPTER 6

MEASUREMENT RESULTS

The converter is implemented in 45-nm digital CMOS technology. Single poly and 7 metal layers are used in this design. Figs. 6.1 and 6.2 show the full layout and die photo outlining the critical parts. The total silicon area is 3.036 mm^2 (1.65 mm × 1.84 mm) excluding the pad-frame, where 2.64 mm^2 (87% of the total area) is occupied by the 1.8-V rated output capacitors, while the input/output power switches, routing, and control circuits are occupying only 0.4 mm^2. The choice of the output capacitors was driven by the desire to minimize leakage and enabling higher than 1.2-V outputs at the expense of silicon area (1.2-V rated capacitors would occupy about half the area of the 1.8-V rated capacitors).

The dynamic and cross-regulation performance of the converter is measured by applying a periodic half-to-full load step to one of the 15-mA outputs (3^{rd} output) as shown in Fig. 6.3, while all the other outputs are at their half loads. As shown, the settling time of the 3^{rd} output is only 30 ns with no overshoot or undershoot observed in response to the applied load step, and all the other outputs show no cross-coupling transients. The absence of observable overshoot or undershoot and cross-coupling transients is owed to the combination of comparator-based control, freewheeling current reserve, and fast output switching frequency. The steady-state DC offset error (50 mV) on the 3^{rd} output with the load level change is primarily due to the comparator-based output control. These controllers are ripple-based controllers, i.e. they regulate either the peak or valley of the output voltage rather than its average. Therefore, as the load level changes, the average output voltage will change with it. Besides, the reason for different peak

values in comparator-based control SIMO converters is due to the change of the comparator delay. This change is determined by the magnitude of the current step relative to the full load value of the output, and not by the absolute value of the current step itself. Therefore, the delay of the comparator will be longer at lighter loads (because the ripple is smaller, leading to smaller comparator overdrive, and thus longer comparator delay). As a result, the peak of the output voltage will increase, which effectively results in a higher average output voltage level than at heavier loads, and this is the second reason for the DC voltage offset on the output voltage. These are typical limitations to output comparator-based controller in general. The same behavior can also be seen in Figs. 15(a) and 4.3.5 of references [14] and [18] respectively. Since this design is for "low-power" applications, the load step by definition is small (7.5 mA) compared to other high-power SIMO implementations, which makes the absolute DC load regulation ($\Delta V/\Delta I$) look worse due to the smaller ΔI. However, if the full-load current is much larger, the absolute value of the DC load regulation is actually very similar to other published work [14], [18] because ΔV stays the same while ΔI would be larger. ΔV stays the same because the size of the output capacitors in SIMOs must be scaled based on the full-load value of the outputs in order to obtain the same voltage ripple, and thus there is no change of the comparator delay. Moreover, the IR drop between the measurement point on the PCB where the load step is being applied and the internal feedback node that the controller is regulating contributes to that offset as well. A zoom-in steady-state voltage ripple waveform for one of the outputs is also included in Fig. 6.3. All the other outputs have similar ripple magnitude (lower than 80 mV). The DVS performance of the converter is measured by applying a ±0.6-V step request to the 50-mA output used for the digital core (5^{th} output) while all the other outputs are at their maximum loads. As shown in Fig. 6.4(a), the output responds within 80 ns for the positive step and within

160 ns for the negative step with no observable cross-coupling transients on all the other outputs. It is worth noting that the response to the negative step is determined by the load current to discharge the output holding capacitor rather than the converter. To demonstrate the impact of the freewheeling current on the dynamic performance of the converter, the same DVS measurements are repeated with various freewheeling current settings in Fig. 6.4(b). As expected, lower freewheeling current results in slower response.

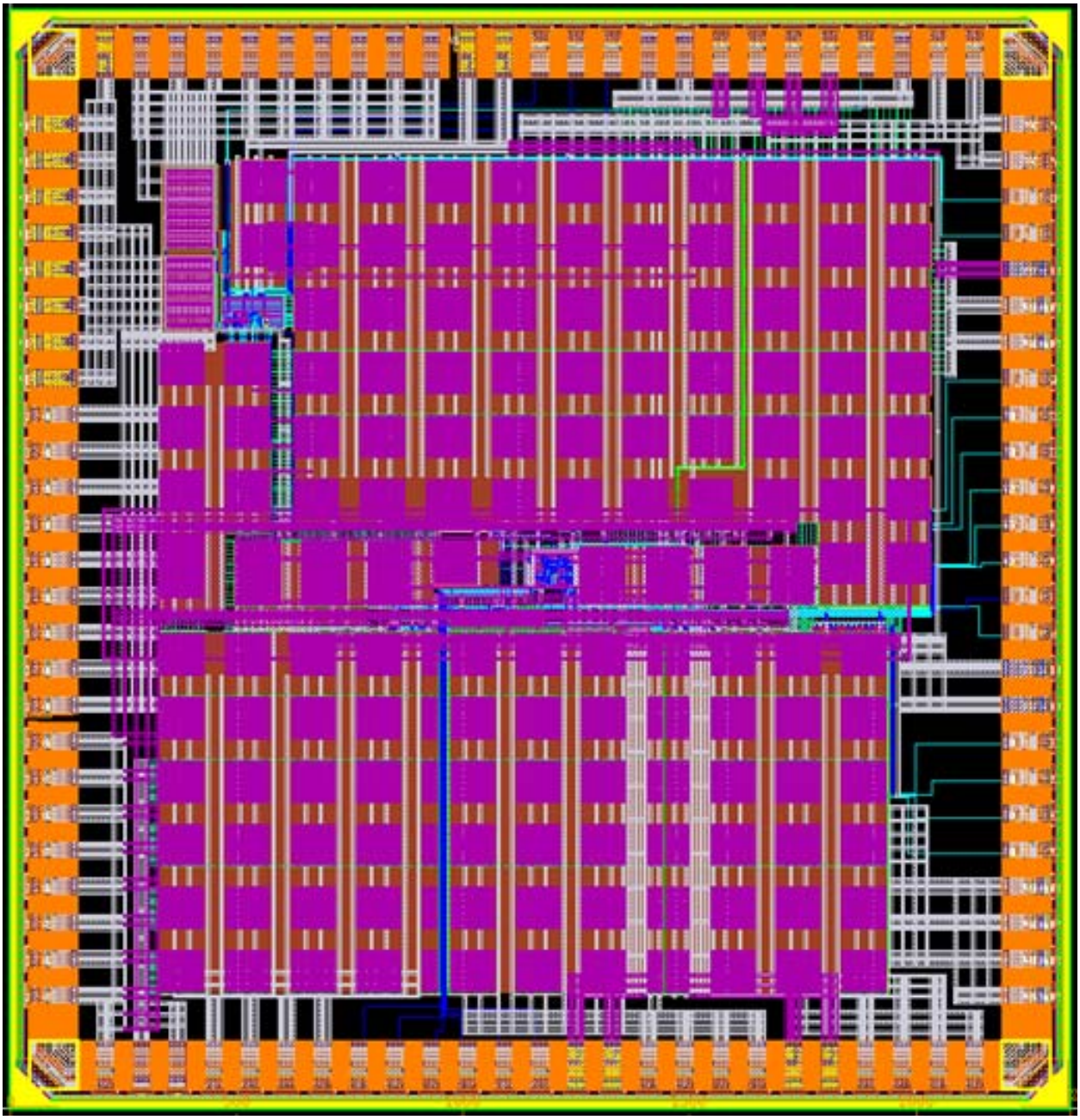


Figure 6.1. Layout of the proposed DF-SIMO buck converter in 45-nm CMOS technology.

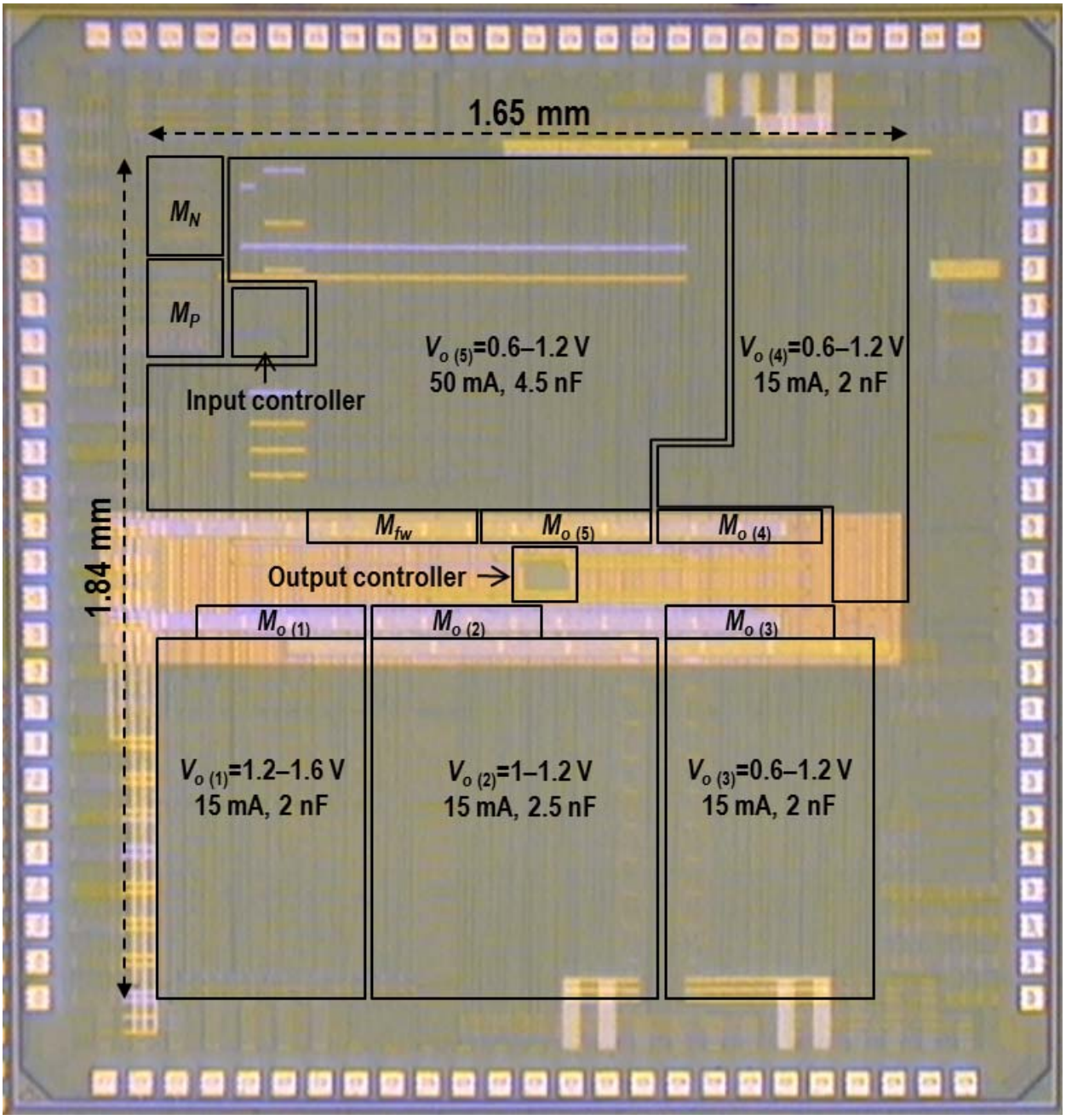


Figure 6.2. The die photo of the proposed DF-SIMO buck converter showing the key blocks.

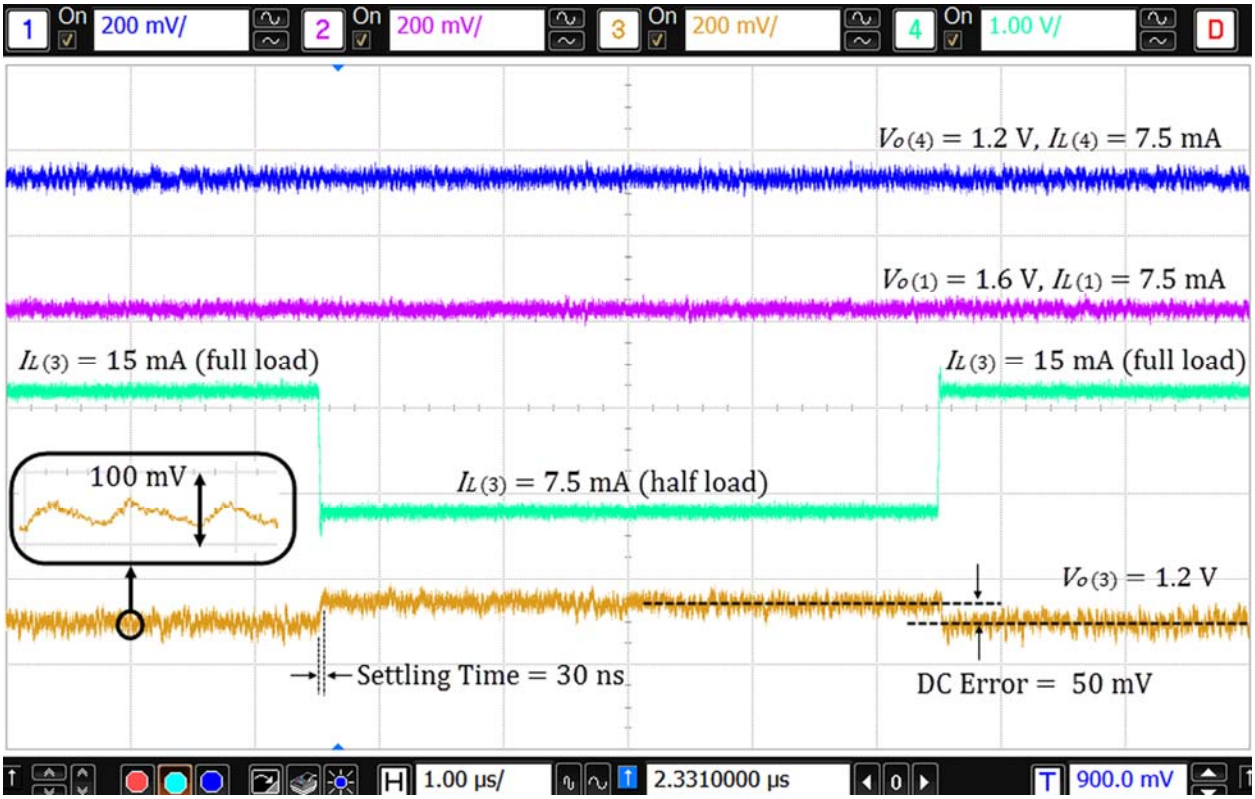


Figure 6.3. Measured dynamic performance of the proposed DF-SIMO buck converter with a half-to-full load step (±7.5 mA) at the 3rd output while all the other outputs are at their half loads.

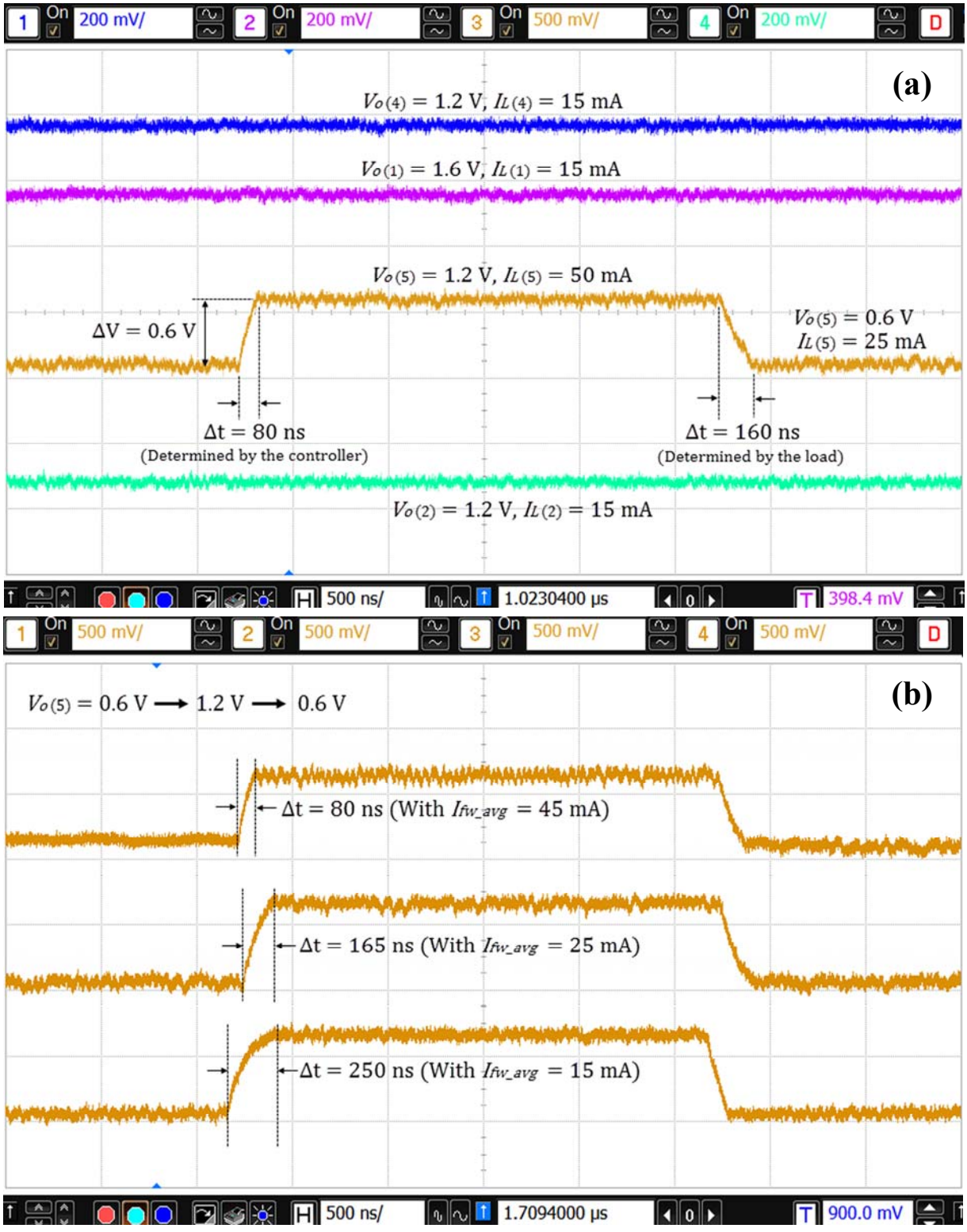


Figure 6.4. Measured DVS performance at the 5th output with all the other outputs at their full loads: (a) with 45-mA freewheeling current, and (b) performance comparison with different freewheeling current settings.

The overall measured and simulated efficiency of the converter versus output voltage and load current under various conditions are shown in Figs. 6.5, 6.6 and 6.7. These measurements do not include the power consumption of the 2-MHz and 120-MHz input and output clocks as they are provided externally as shown in Fig. 6.10. However, a 120-MHz clock is relatively slow in a technology such as 45 nm, and its power consumption (<100 μW) is very small to make any noticeable difference in the efficiency. Additionally, high-frequency clocks are readily available in many target SoCs, which can be used for the power converter without any additional power overhead. The measured peak efficiency, which occurs at full load, is 73%, while the expected peak efficiency from simulations is 83.5%. The difference between the simulated and measured efficiency at full load is dominated by the excessive parasitic resistances of the on-chip input and output power routing ($\sim$0.82 Ω and $\sim$0.25 Ω respectively), which caused substantial additional conduction losses as outlined in the loss breakdown in Table 6.1. This can be significantly reduced in order to approach the simulated values with better power bus layout and placement of the input/output power switches, which have not been done as well as they should due to tight fabrication deadline and last minute layout changes to meet the metal density rules. However, if this 10% difference in simulated and measured efficiency is simply caused by excessive conduction losses across the power routing, then we should see that this difference in efficiency shrinks at lighter load currents because conduction losses drop as the load current drops ($I^2 \times R$), which is exactly what we can observe comparing the two simulated curves (schematics only vs. schematics with routing resistances) in Fig 6.7. But why the measurement results do not agree with this hypothesis? The reason is that the routing resistances only explain 8% of the 10% difference in efficiency at full load, while the remaining 2% is because of the additional switching and transitional losses across the power switches due to the degraded rise/fall times of

the control signals post layout. Now, as the load current drops, these additional switching losses are not scaling with the load and start to have a more significant contribution to the difference in efficiency as the conduction loss portion scales down. So essentially it offsets the benefit of the drop in conduction losses across the routing resistors. And this is why the difference between simulation (schematics only) and measurement continues remaining more or less the same at lighter load conditions.

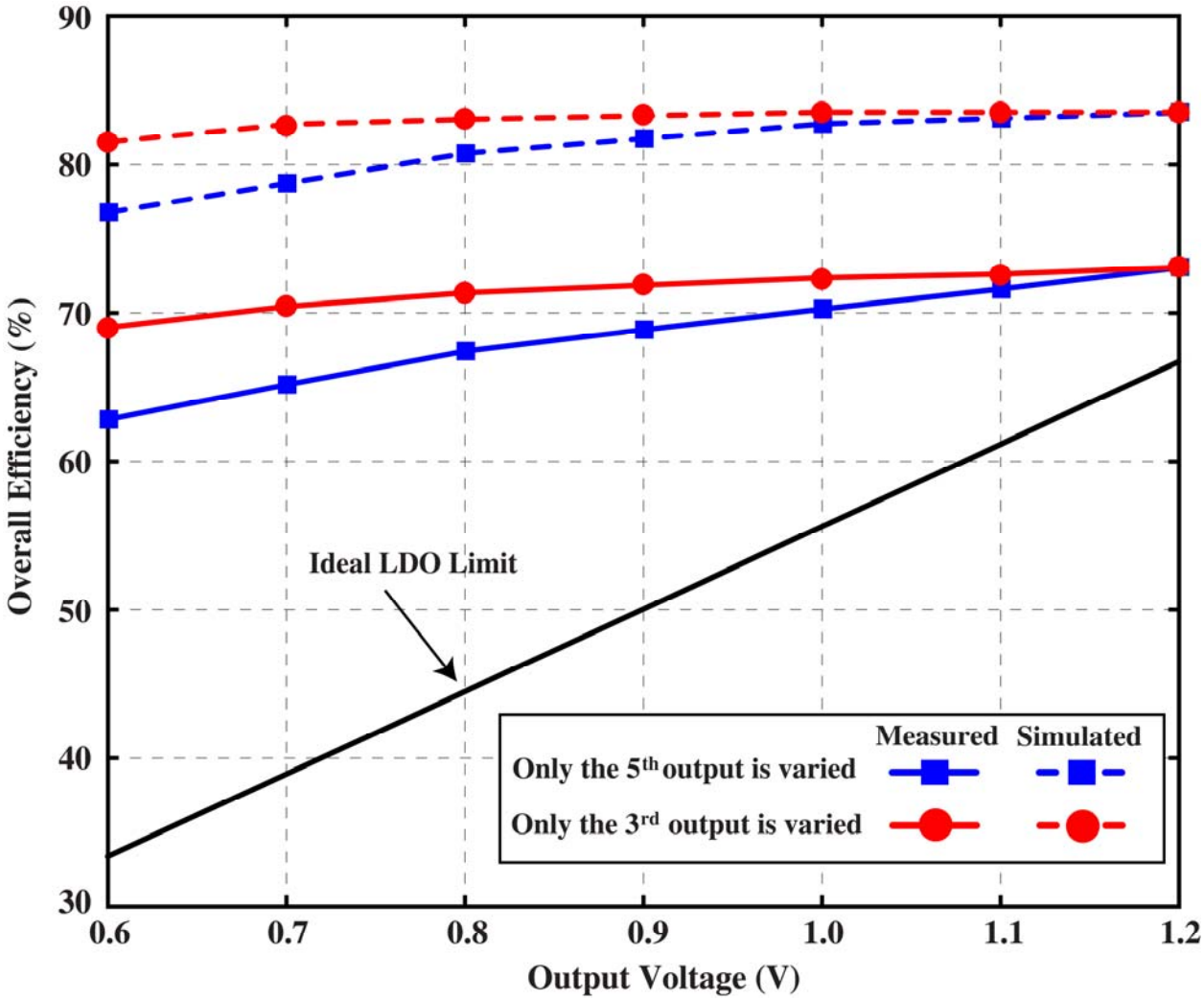


Figure 6.5. Measured and simulated overall efficiency of the converter versus the output voltage of the 5th output while all other outputs are at their maximum power, and versus the output voltage of the 3rd output while all other outputs are at their maximum power.

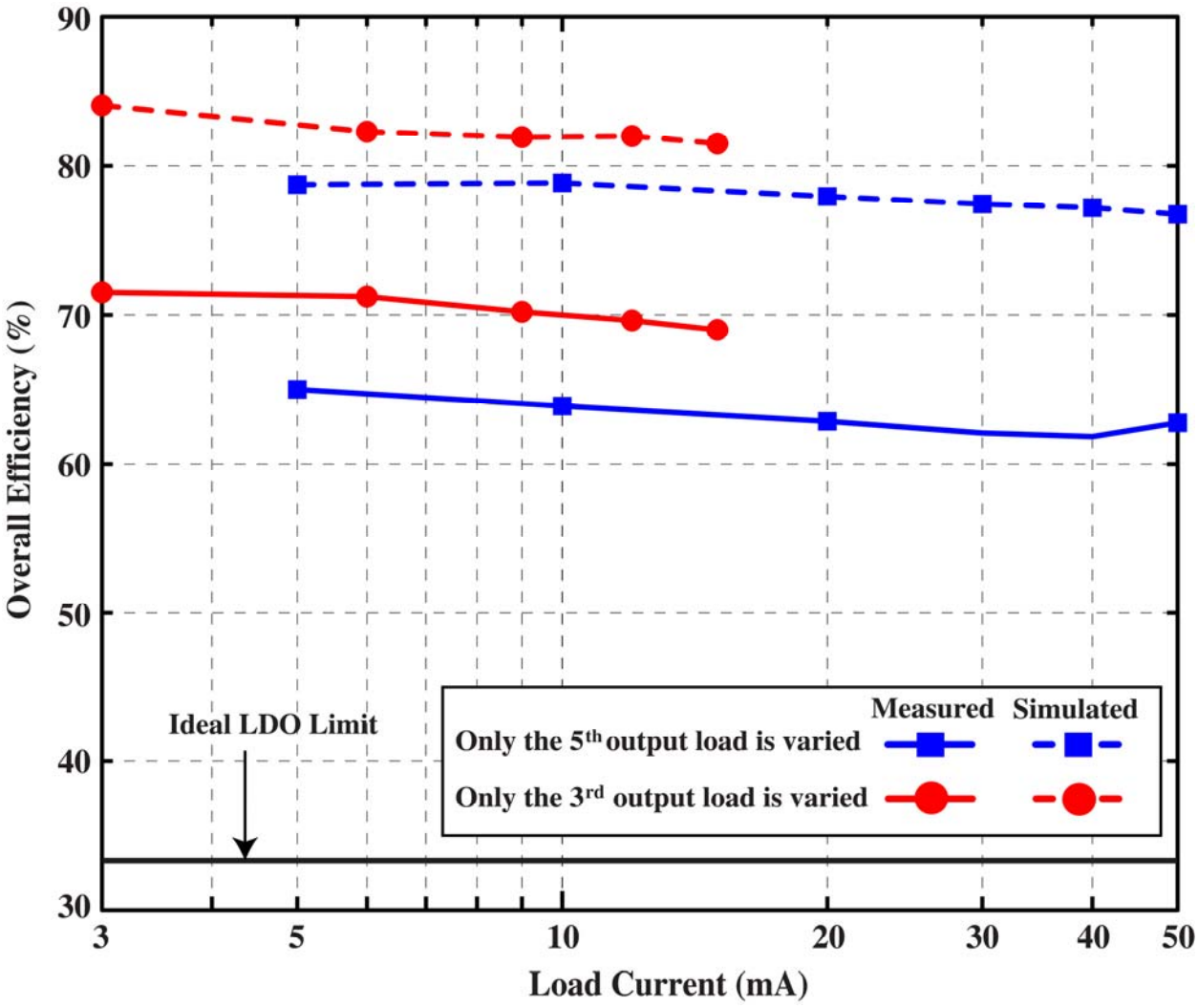


Figure 6.6. Measured and simulated overall efficiency of the converter versus load current when the load current of either the 5th or the 3rd output at 0.6 V is varied while all other outputs are at their maximum power.

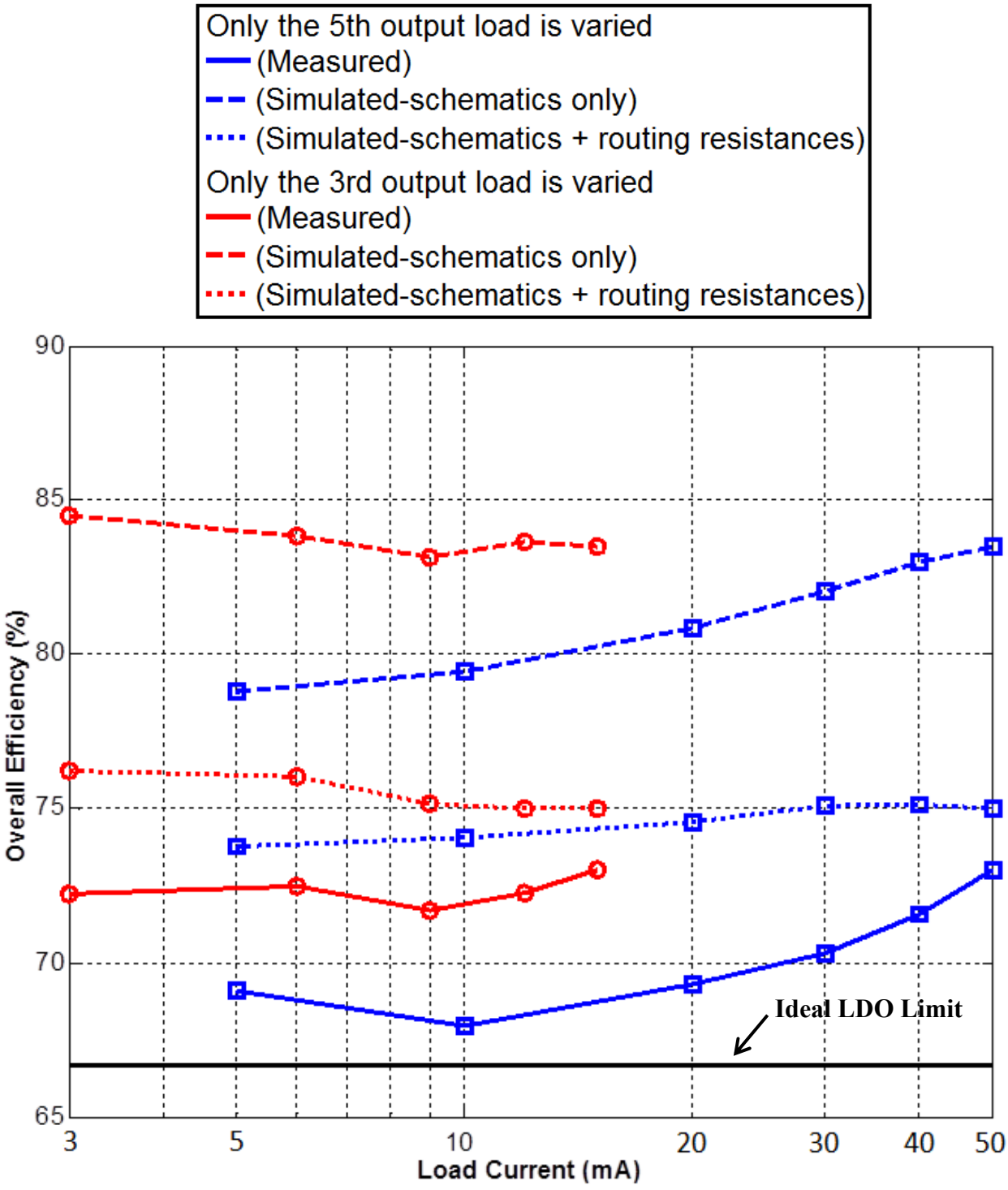


Figure 6.7. Measured and simulated overall efficiency of the converter versus load current when the load current of either the 5th or the 3rd output at 1.2 V is varied while all other outputs are at their maximum power.

Table 6.1. Losses breakdown at maximum rated power.

	Losses and their relative percentage of total loss								Total loss	Total output power	Efficiency
	Input stage			Inductor DCR (37 mΩ)	Output stage			Control circuits (Quiescent loss)			
	FETs switching loss	FETs conduction loss	*Routing loss		FETs switching loss	FETs conduction loss	*Routing loss				
Simulated (Schematics only)	0.7 mW (2.6%)	3.7 mW (13.7%)	0	0.6 mW (2.1%)	8.4 mW (30.8%)	10.6 mW (38.8%)	0	3.2 mW (11.9%)	27.3 mW	138 mW	83.5%
Simulated (Schematics, including input & output routing)	0.7 mW (1.6%)	4.7 mW (10.2%)	13.8 mW (30%)	0.6 mW (1.3%)	8.4 mW (18.3%)	10.5 mW (22.8%)	4 mW (8.7%)	3.3 mW (7.1%)	46 mW	138 mW	75%
Measured	21.2 mW (41.6%)			0.8 mW (1.6%)	6.9 mW (13.5%)	19 mW (37.3%)		3 mW (5.9%)	51 mW	138 mW	73%

* Includes on-chip power routing, and package parasitics

The measured input stage switching node, inductor current, and output stage switching node in steady-state operation are shown in Fig. 6.8 for 2-MHz and 50-MHz input and output switching frequencies respectively. The reason I had to reduce the output switching frequency is because the probes I have available for doing the measurement have only 200-MHz bandwidth as shown in Fig. 6.9. Although this is enough bandwidth to accurately capture all the nodes in the converter (including the outputs), it is not enough for getting a clear waveform of the output switching node because that node has sharp transitions between the various output levels (much higher frequency components than the fundamental 120-MHz switching). With only 200-MHz probe bandwidth, the output switching node looks like a distorted sine-wave because all the higher frequency components of the signal that correspond to the sharp transitions are filtered out. To circumvent this limitation and to get an output switching node waveform that is illustrative of the theory and is clear enough to show the transitions, I had to drop the output switching frequency to 50 MHz for the purpose of this particular measurement ONLY. All other measurements in this chapter are done with 120-MHz output switching frequency. Nonetheless, the waveform clearly shows the expected behavior at the output switching node. Unfortunately, this is the best I can do at this time to address this measurement because purchasing a higher bandwidth probe to enable capturing this node with its sharp transitions while keeping 120-MHz frequency is not possible for me at this time. Table 6.2 summarizes the key performance metrics of the converter, along with a comparison with previous literature.

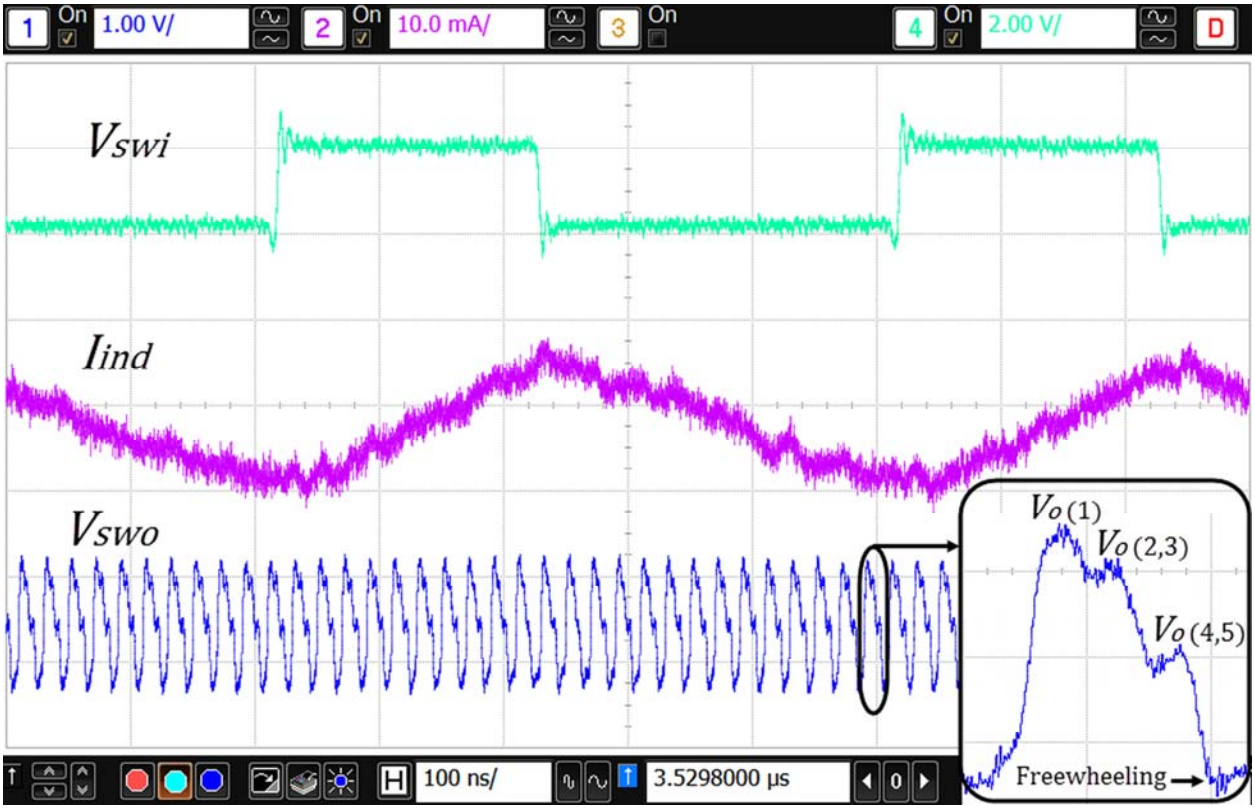


Figure 6.8. The measured input switching node, inductor current, and output switching node with 2-MHz input switching frequency and 50-MHz output switching frequency.

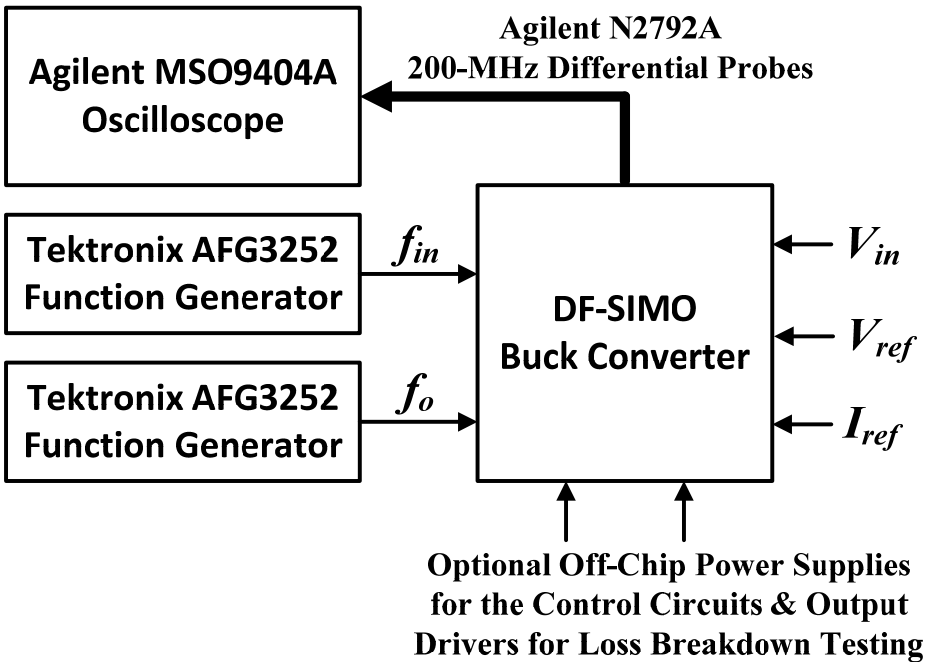
Figure 6.9. Agilent N2792A 200-MHz differential probe used for measurement.

Table 6.2. Performance summary & comparison.

		This Work	ISSCC 2014 [18]	ISSCC 2012 [17]	ISSCC 2010 [15]	JSSC 2008 [16]
Technology		45-nm CMOS	0.35-μm CMOS	65-nm CMOS	0.35-μm CMOS	0.5-μm BiCMOS
Topology		DF-SIMO (Buck)	SIMO (Buck)	SIMO (Buck)	SIMO (Buck)	SIMO (Boost)
# of Outputs		5	4	5	6	2
Input Voltage Range		1.6–2.0 V	2.7–5 V	3.4–4.3 V	5 V	2.7–4.5 V
Output Voltage Range		0.6–1.2 V (3 outputs) 1–1.2 V (1 output) 1.2–1.6 V (1 output)	0.9 V, 1.2 V 1.5 V, 1.8 V (Range is not reported)	1.2 V, 1.5 V 1.8 V, 2.5 V, 2.8 V (Range is not reported)	1 V, 1.3 V, 1.6 V 2 V, 1.9 V, 3 V (Range is not reported)	4 V, −4.8 V (Range is not reported)
Maximum Load (Total)		110 mA	1.6 A	1.15 A	698 mA	200 mA
Switching Frequency		2 MHz (Input stage) 120 MHz (Output stage)	1 MHz (Single frequency)	1.2 MHz (Single frequency)	2 MHz (Single frequency)	0.8 MHz (Single frequency)
Inductor Range		10–15 μH	4.7 μH	2.2 μH	4.7 μH	10 μH
Output Capacitors		2 nF/output (3 outputs) 2.5 nF (1 output) 4.5 nF (1 output) All On-Chip	10 μF/output Off-Chip	4.7 μF/output Off-Chip	10 μF/output Off-Chip	10 μF/output Off-Chip
Silicon Area		3.04 mm^2 (2.64 mm^2 of that is for the output capacitors)	5.4 mm^2	1.86 mm^2	7.5 mm^2	3.22 mm^2
Maximum Output Voltage Ripple		80 mV	30 mV	40 mV	25 mV (500 mV with spikes)	100 mV
Peak Efficiency		73% (Measured) 83.5% (Simulated)*	87%	83%	Not Reported	81%
DVS		+0.6 V/0.08 μs −0.6 V/0.16 μs	+0.6 V/10 μs −0.6 V/25 μs	Not Reported	Not Reported	Not Reported
Load Transient Response	**Load Step (ΔI_L)**	Half-to-Full Load (ΔI_L = 7.5 mA)	1/4-to-7/8 Full Load (ΔI_L = 250 mA)	~1/4-to-7/8 Full Load (ΔI_L = 150 mA)	~1/4-to-Full Load (ΔI_L = 81 mA)	No-to-Full Load (ΔI_L = 100 mA)
	Overshoot / Undershoot	None was observed*	40 mV	40 mV	Not Reported	120 mV
	Settling Time	0.03 μs	7 μs	100 μs	150 μs	20 μs
	Cross Regulation	None was observed*	0.04 mV/mA	0.067 mV/mA	Not Reported	Not Reported

*** See chapter 6 for details regarding the simulated versus measured efficiency, as well as the load transient response of the converter.**

This work is packaged with 100-pin TQFP for testing, but better packages (e.g. QFN) could be chosen to reduce the parasitics and further improve the performance. Fig. 6.10 shows the measurement setup and the test board. The model numbers of all the test equipment I used are also indicated. In the current design, I_{fw_ref} is simply provided to the chip by the test equipment (a reference current generator) so I can manually change it to test the design with various freewheeling current levels. In an actual product, this reference current will likely be generated by a bandgap and a reference resistor. Moreover, as I discuss in section 3.2.2, it is possible to have I_{fw_ref} adapted to anticipated load changes to improve transient response, but this is not something that I implemented in this particular testchip. As for the input and output switching frequencies, it is important to note that there is no special timing requirement on the relationship between them when f_o is much larger than f_{in}. In this implementation, both switching frequencies are actually provided from two off-chip clock sources (test equipment). In an actual product, the output switching frequency may be generated from a simple oscillator, or a PLL if readily available in the SoC, and then it can be divided down as necessary to obtain the input switching frequency. Although this will synchronize the two frequencies and ensure an integer multiple between them, this is not a requirement of the DF-SIMO, but it is one simple method to implement the clocks. Besides, the reason I can have the rough losses breakdown in Table 6.1 is because a testmode is built in the design, where the control circuits and the output switch drivers can be powered either internally or externally from the optional off-chip power supplies. By measuring the power consumption from these optional off-chip power supplies, I can roughly separate the switching losses of the output stage from the conduction losses, and I can also separate the power consumption of the control circuits.



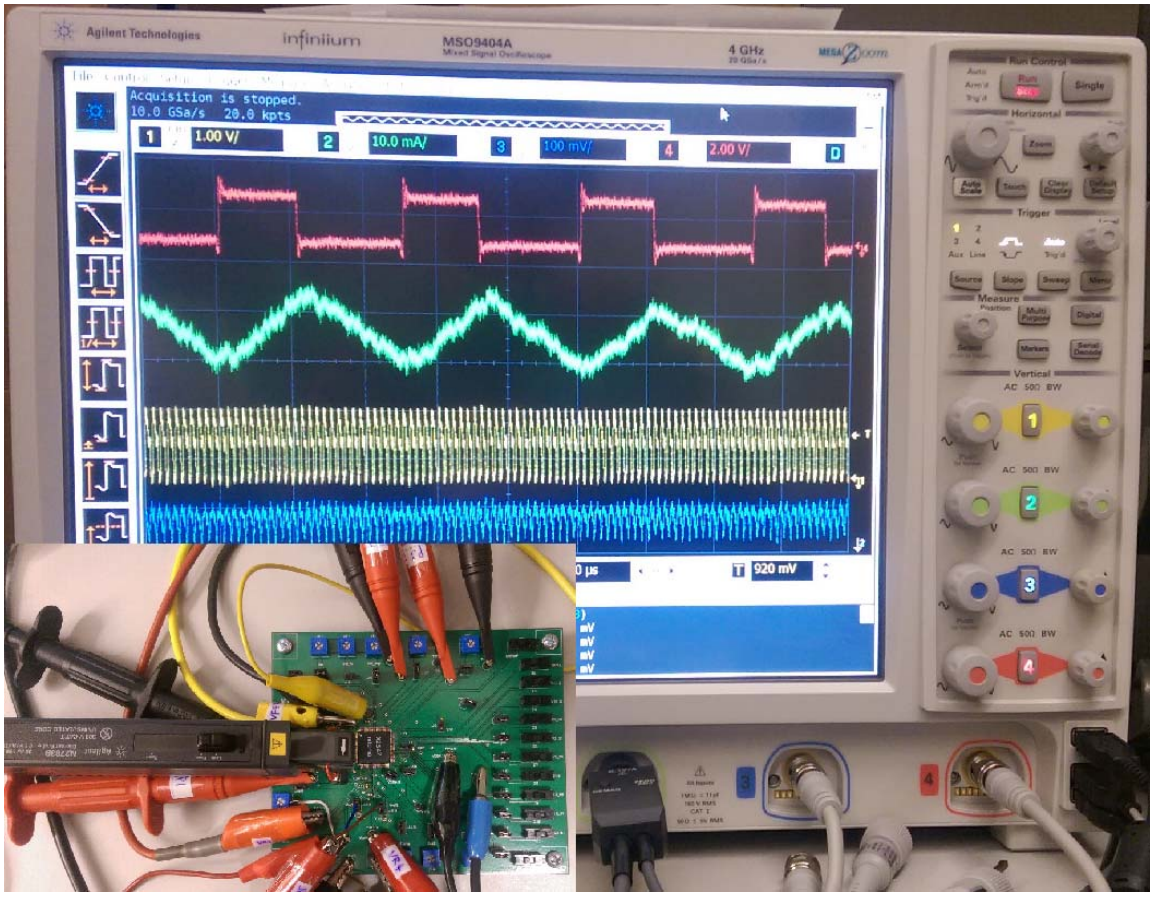


Figure 6.10. Measurement setup used to characterize the proposed DF-SIMO buck converter.

CHAPTER 7

CONCLUSION AND FUTURE EXTENSION

This thesis introduces a first-ever DF-SIMO topology, where the output switching frequency is higher than the input switching frequency. Along with output comparator-based control and freewheeling current PWM control, the topology yields improved dynamic and cross regulation behavior and reduced output capacitors compared to conventional single-frequency SIMO topologies. For output switching frequencies beyond 100 MHz, the output capacitors can be integrated on-chip. Although a low-power DF-SIMO buck converter is demonstrated, the dual-frequency idea can be used to implement low/high-power single/multiple-output buck/boost converters with different control schemes for any applications. The following subsections will suggest some possible designs for future extension.

7.1 Battery-Connected DF-SIMO Power Converters

A common power scheme for mobile applications is to first generate intermediate shared power supplies from battery, and then use subsequent switching converters or low-dropout regulators (LDOs) to provide the large number of low-voltage power supplies required by the SoCs. As the system depicted in Fig. 1.1 in chapter 1, this 1.8-V supply is actually came from another inductor-based power converter. Since this scheme is fundamentally a two-step regulation approach with an intermediate voltage rail, the overall efficiency is the product of the individual efficiency of each regulation step. Therefore, extra losses due to cascading power

supplies are inevitable. However, although the DF-SIMO implementation in chapter 5 is powered by the 1.8-V supply to demonstrate the proposed topology, it can be easily modified to connect to battery directly with minimum design efforts and efficiency impacts because of its low switching frequency characteristic on the input stage as explained in section 3.2.3. Thus a higher overall efficiency is reasonably expected for this one-step regulation approach.

7.2 High-Power DF-SIMO Converters with Bondwire-Based Output Filters

As discussed in section 3.2.1, there is a tradeoff between the output capacitors and voltage ripple for a given output switching frequency. In order to provide higher full-load current and maintain similar voltage ripple, the size of the output holding capacitor should be scaled up. However, to implement a high-power DF-SIMO buck converter may require significant die area simply for the output capacitors which offsets the purpose of integrating them to reduce the overall cost. For example, if a maximum load of 200 mA is required for one output with a 100-MHz output switching frequency, based on Eq. (3.2), an output capacitance larger than 30 nF is needed to maintain around 50-mV output voltage ripple. A 30-nF 1.8-V rated MOS capacitor occupies more than 7 mm^2 die area, which is not cost-effective and practical for nanometer technology nodes. Hence, to improve the power density, two possible options are suggested here for future extension. First, these output capacitors can be made with higher density, lower leakage and lower cost on a conventional technology, and then stacked and connected to the lower chip made on an advanced technology like 45-nm CMOS. This stacked-chip implementation for output filter is already demonstrated in [39] for a conventional single-output buck converter. Another method is to utilize the standard package bondwire intrinsic inductance

to form the additional energy storage components for output filtering. Similar idea is presented in [40] as the main power inductor for single-output cases. However, since the inductor current delivered to each output is discontinuous for multiple-output cases, an enhanced fully-integrated bondwire-based output filter structure is proposed here as shown in Fig. 7.1. This low-pass filter is designed to further attenuate the voltage ripple at the output switching frequency. With this configuration, high power density and low overall cost can be achieved at the same time for DF-SIMO converters.

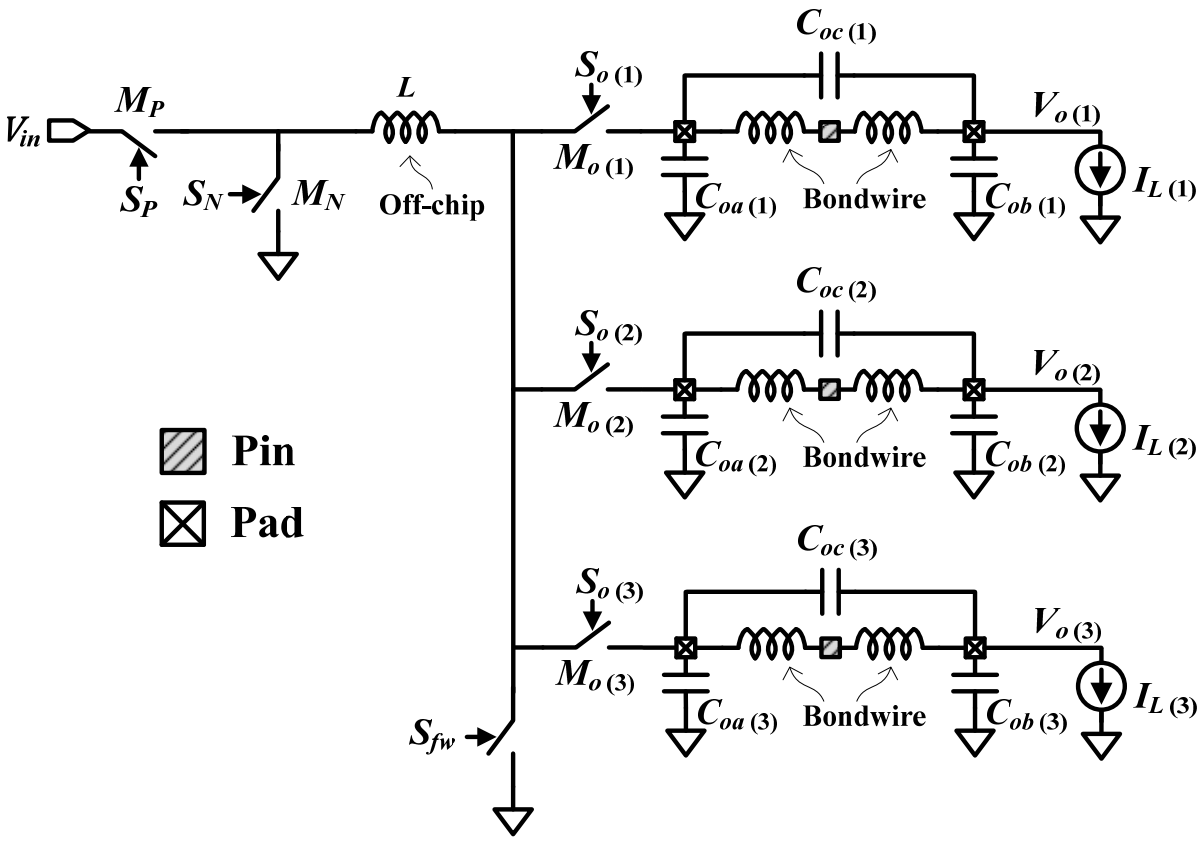


Figure 7.1. Multiple-output buck converters with bondwire-based output filters.

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